Integration Progress and Trends in Miniature Integrated Power Supplies

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Presented by Arnold Alderman

Focus – Integration from the Product View

- Sourcing and management power to processor ICs
- Integration effort began with a selected product:
  - The Power-Supply-in-Package (PSiP)
    - Modular – singular and quad converters with associated power passive(s)
  - The Power-Supply-on-Chip (PwrSoC)
    - Modular – Single converter with power passive
    - Granular – High number of integrated parallel converters
- Potential for higher levels of integration

Commencing the PMU Integration

PMU = Power Management Unit

Optional → Digital

	Control Function	Monitor Function	Status Function	Driver	LDO	MOSFETs
Level 1	Single Contoller IC			Separate IC	Separate LDO	Discrete
Level 2	Multiple Controller ICs			Separate IC	Separate LDO	Discrete
Level 3	Single Controller IC with Integrated Drivers				Separate LDO	Discrete
Level 4	Multiple Controller ICs with Integrated Drivers				Separate LDO	Discrete
	Integrated Regulator(s) with Discrete MOSFETs					Discrete
Level 5	Integrated Regulator(s) with Integrated MOSFETs					

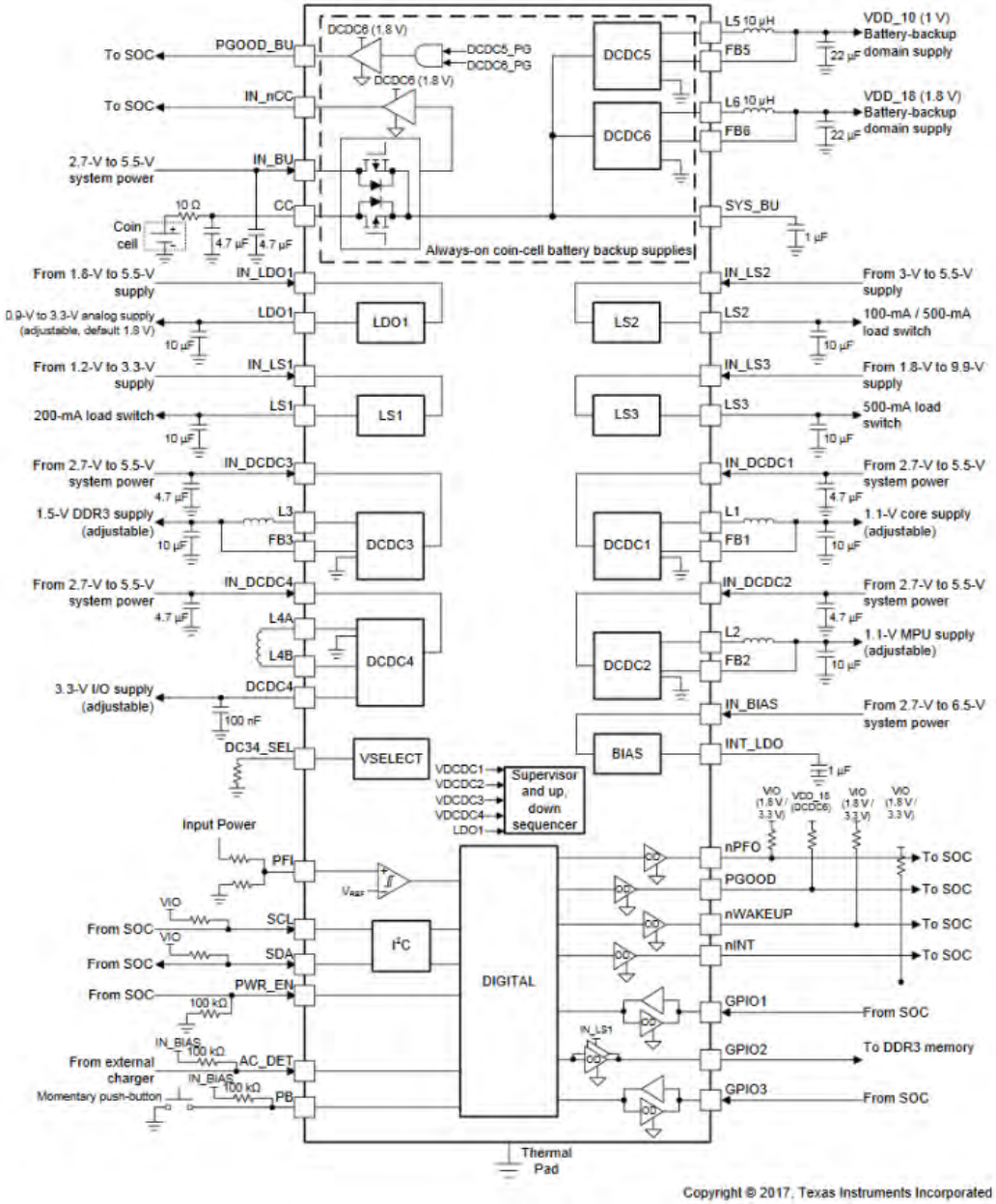
- Tracing controller IC integration needs & growth
- Many loads have multiple power busses to be sourced and managed

The Complex PMU

- Three Adjustable Step-Down Converters With Integrated FETs
  - DCDC1: 1.1-V Default up to 1.8 A
  - DCDC2: 1.1-V Default up to 1.8 A
  - DCDC3: 1.2-V Default up to 1.8 A VIN Range From 2.7 V to 5.5 V Adjustable Output Voltage Range

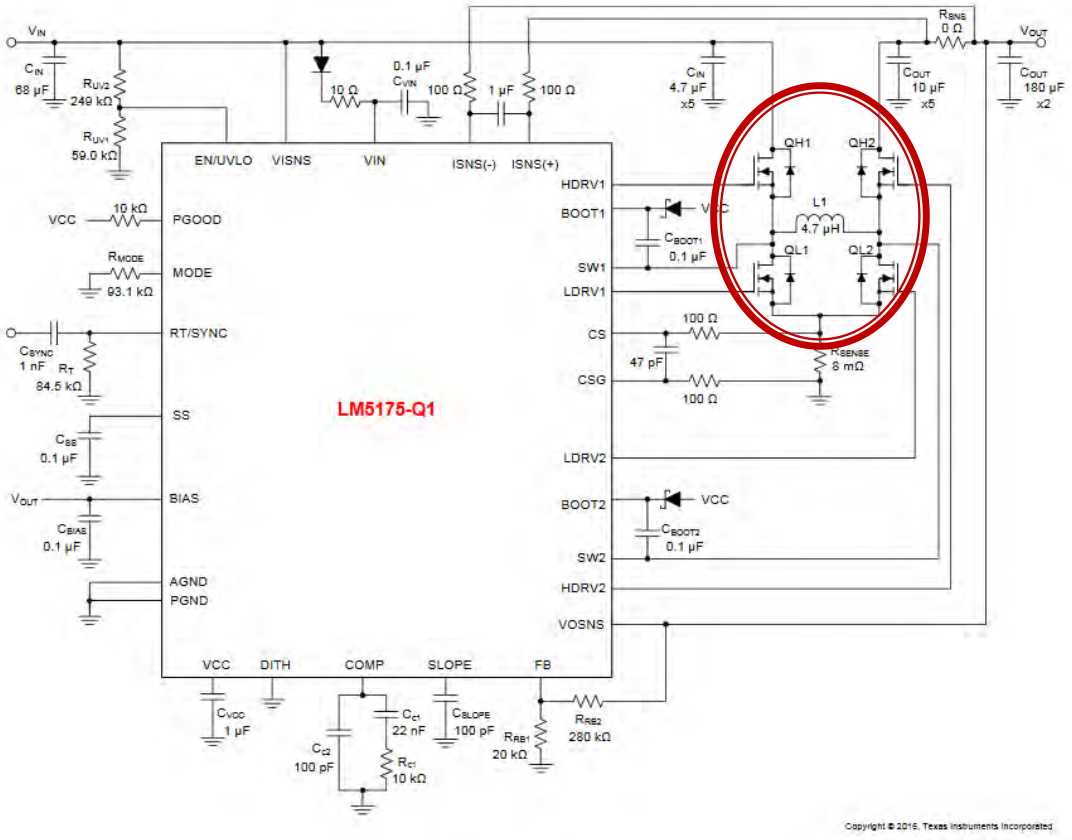
Texas Instruments TPS65218D0

Integrated Power Management (PMIC) for ARM® Cortex™-A8/A9 SOCs and FPGAs



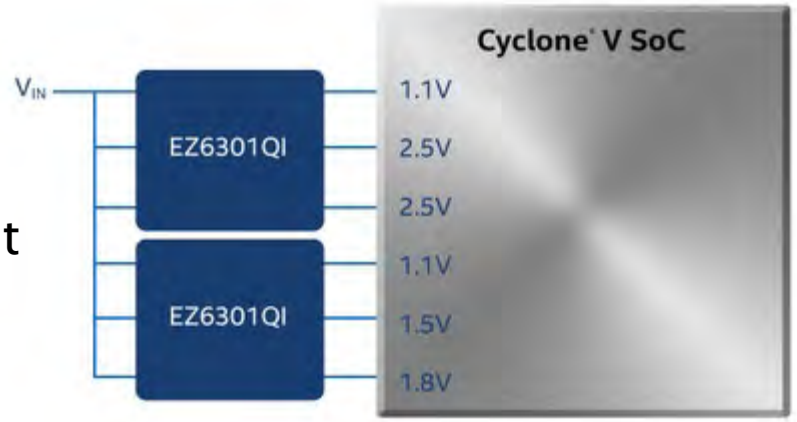
PMUs with external switches

- Adding the lateral power switches
  - Integrated – BDCMOS
- Discrete vertical switches are still preferred in many cases
  - Lateral switches are twice as large as vertical
  - Higher efficiency
  - 2X Higher current density A/mm^2



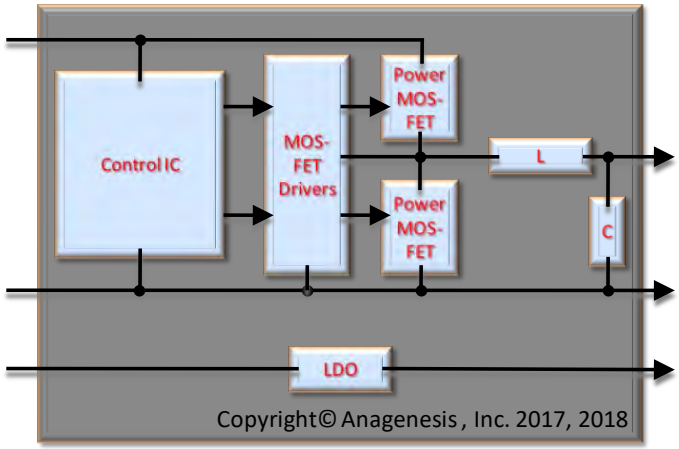
The Power Supply in a Package (PSiP)

- A high current density package integrated power converter having 1" maximum in any dimension with current density of more than 0.004 A/mm^3



Component	Requirement
Controller	Required
Power Switch Drivers	Required
Power Switches	Required
Power Passive	Required (L or C or Both)
LDO	Optional
Digital Control	Optional

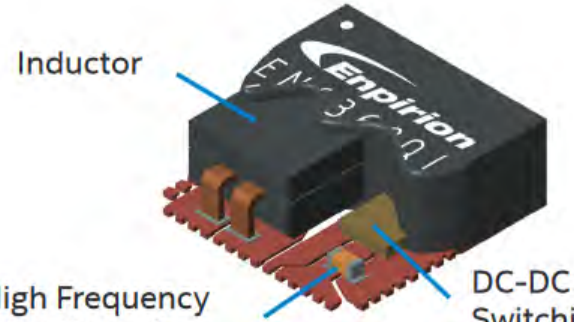
e.g. Used to supply regulated power adjacent to the load (Point-of-Load {POL} power converter)



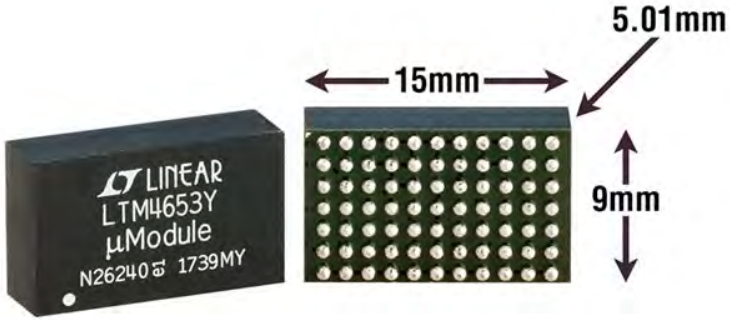
PSiP

Typical PSiPs

- DC-DC converters – over 90% of product base
- Other converters: LED drivers, transceivers, battery chargers…
- Number of suppliers: 25

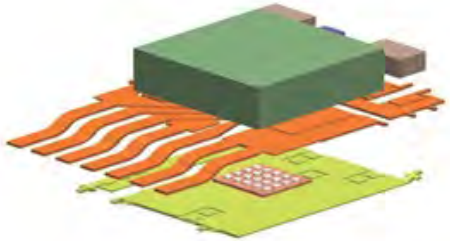


60A, 4.5V to 16V input voltage 0.5V to 1.3V 23mm x 18mm x 5mm QFN package



Encapsulated Organic Substrate Version

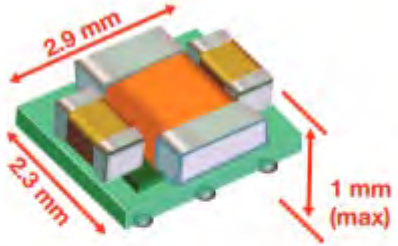
Internal Construction of a Leadframe Encapsulated Version



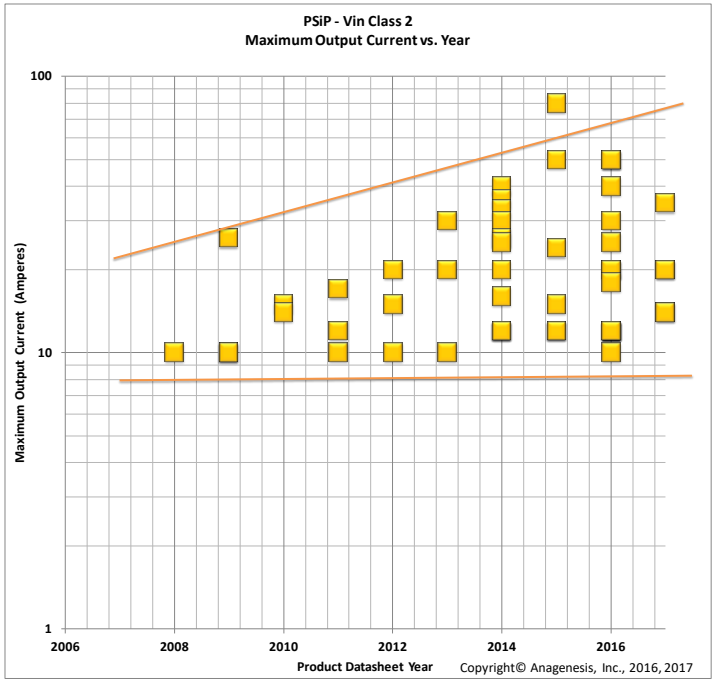
Dual Leadframe Source: Texas Instruments

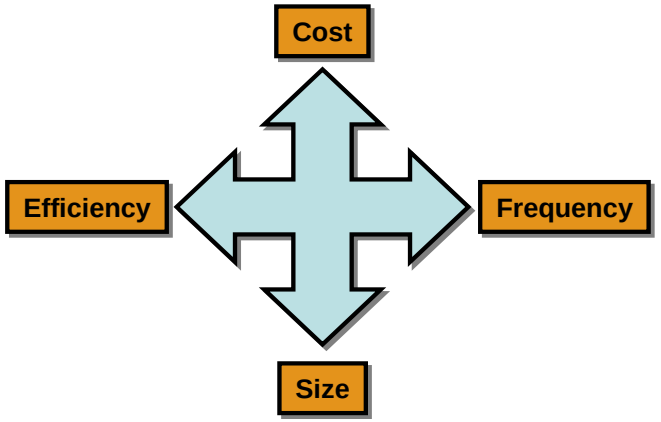
Added external capacitors don't add significantly to the converter foot print.

Miniature Open Constructed Version



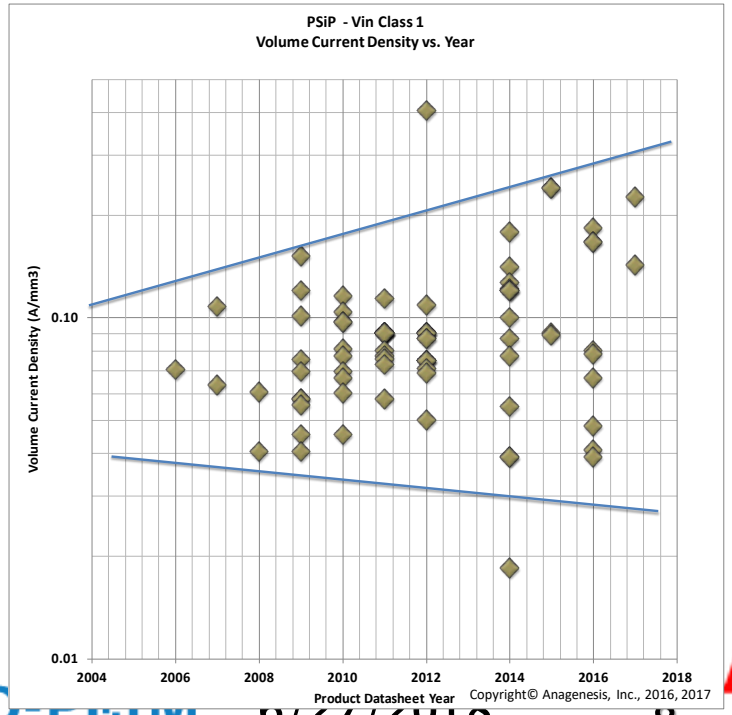
Source: Texas Instruments





The PSiP design tradeoffs

Class-1 volume current density vs. datasheet year with part number identified



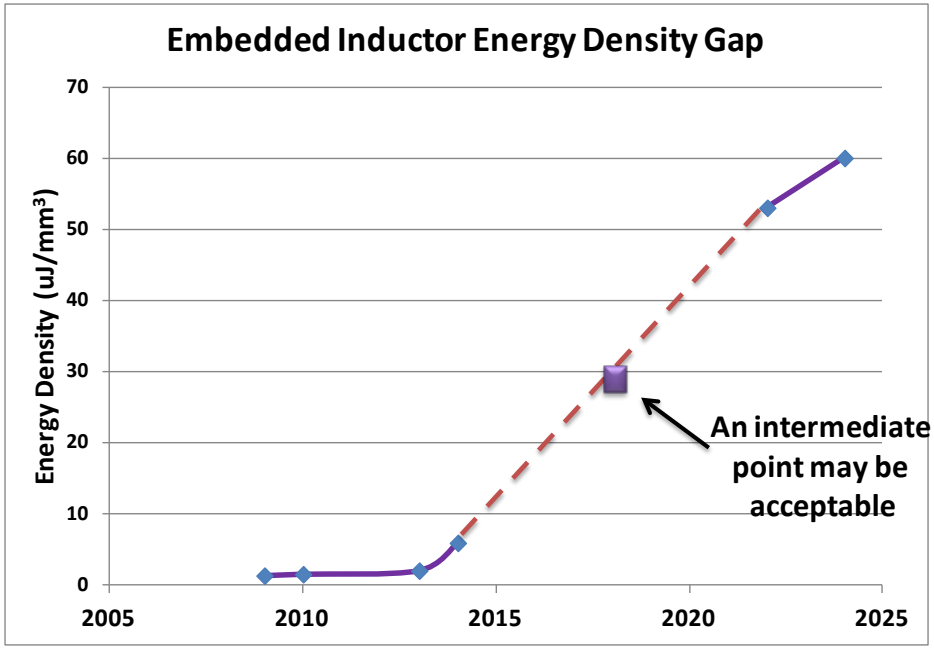
Class 2 products showing the breakdown by maximum-input-voltage

Embedded Power Inductor Gap Analysis

Under Board 3A
Ultra-thin
6.26 x 6.25 x 1.82 MM
But
Embedded Would Be An Improvement

Embedded L Target	
Parameter	Target Value
Inductance	0.5 µH
Power	50 W Converter
Current Rating	50 Amperes
Frequency	50 MHz
Package	2512 Package
L & W	(6.3 X 3.1 mm)
Thickness	0.6 mm
Energy Density	53.3 µJ/mm^3
Target Date	by 2022

Target Embedded Inductor Parameters year 2022 [1]



Gap Analysis for the Embedded Inductor [1]

Embedded Power Capacitor

Embedded C Target	
Parameter	Target Value
Capacitance	100
Power	50 W Converter
Voltage Rating	25 Volts
Frequency	50 MHz
Package	1206
L & W	(3.2 X 1.6 mm)
Thickness	0.95 mm thick
Energy Density	6424 µJ/mm3
Target Date	by 2022

Table 10 – Target Embedded Capacitor Parameters year 2022 [1]

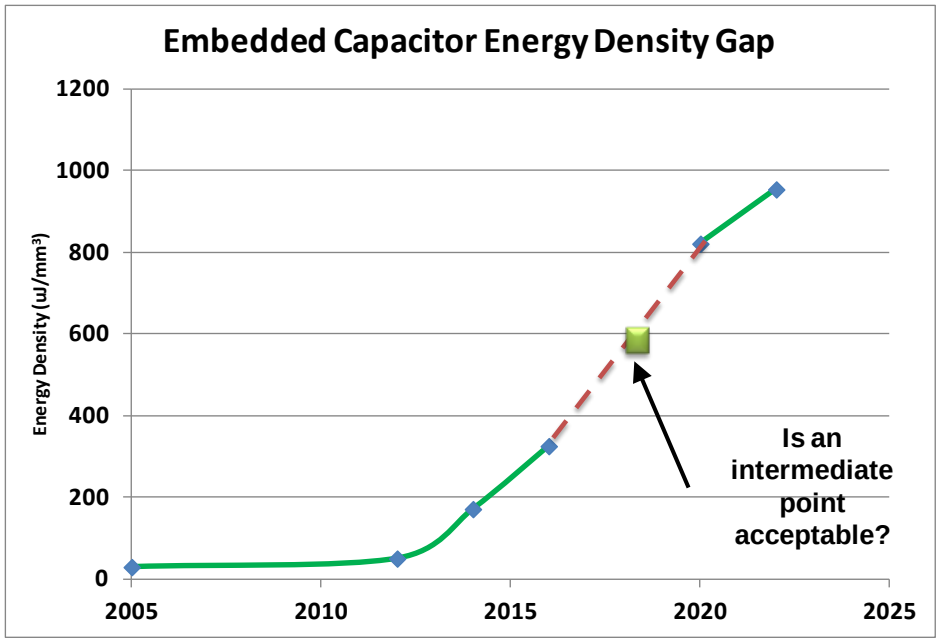
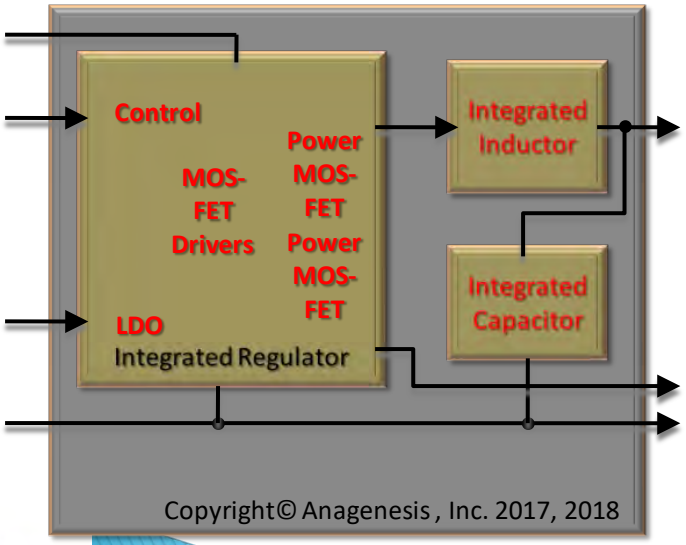


Figure 58 – Gap Analysis for the Embedded Capacitor [1]

Early thoughts…

PwrSoC – Modular Chip Integration

- Physical boundaries similar to the PSiP
- **All elements are integrated into a semiconductor substrate(s) for high volume low cost or to meet challenging power density or system performance requirements**
- A high current density package integrated power converter having 1" maximum in an dimension with current density of more than 0.004 A/mm^3



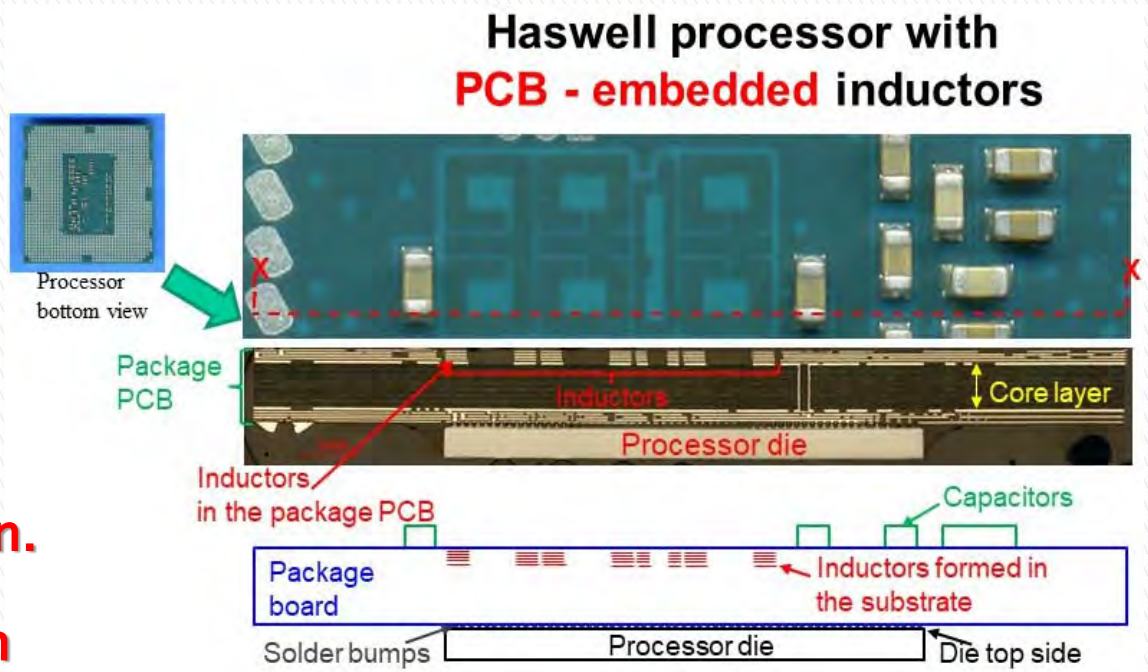
Component(s) on Chip	Requirement
Controller	Required
Power Switch Drivers	Required
Power Switches	Required – can be on separate chip
Power Passive	Required (L or C or Both)
LDO	Optional
Digital Control	Optional

PwrSoC – Granular Chip Integration

All elements are integrated into a semiconductor substrate(s) for high volume low cost manufacturing

Comprised of many "grain" converters to create a single regulator output

The Intel Fully Integrated Voltage Regulator (FIVR) almost satisfies the definition. Deviation: Inductor is on organic substrate rather than inorganic substrate



Haswell processor, partial bottom view and cross-section of the Package substrate.
Source: LTEC Corporation [2]

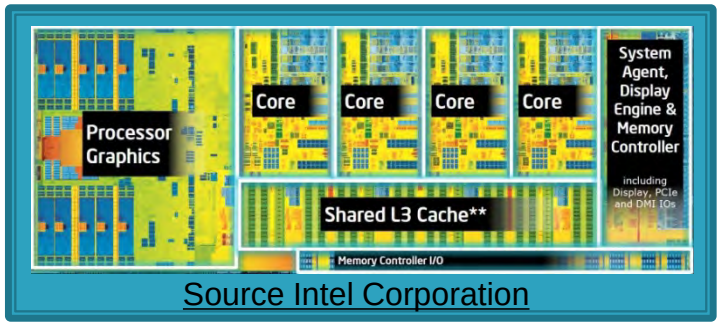
Ferric Approach

Ferric Technology ➡ TSMC Magnetic Cells ➡ Dialog Semiconductor PwrSoC

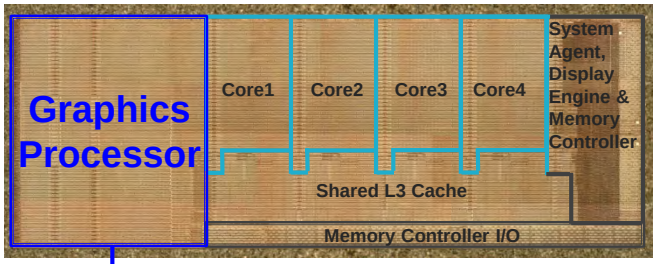
Could be Modular or Granular

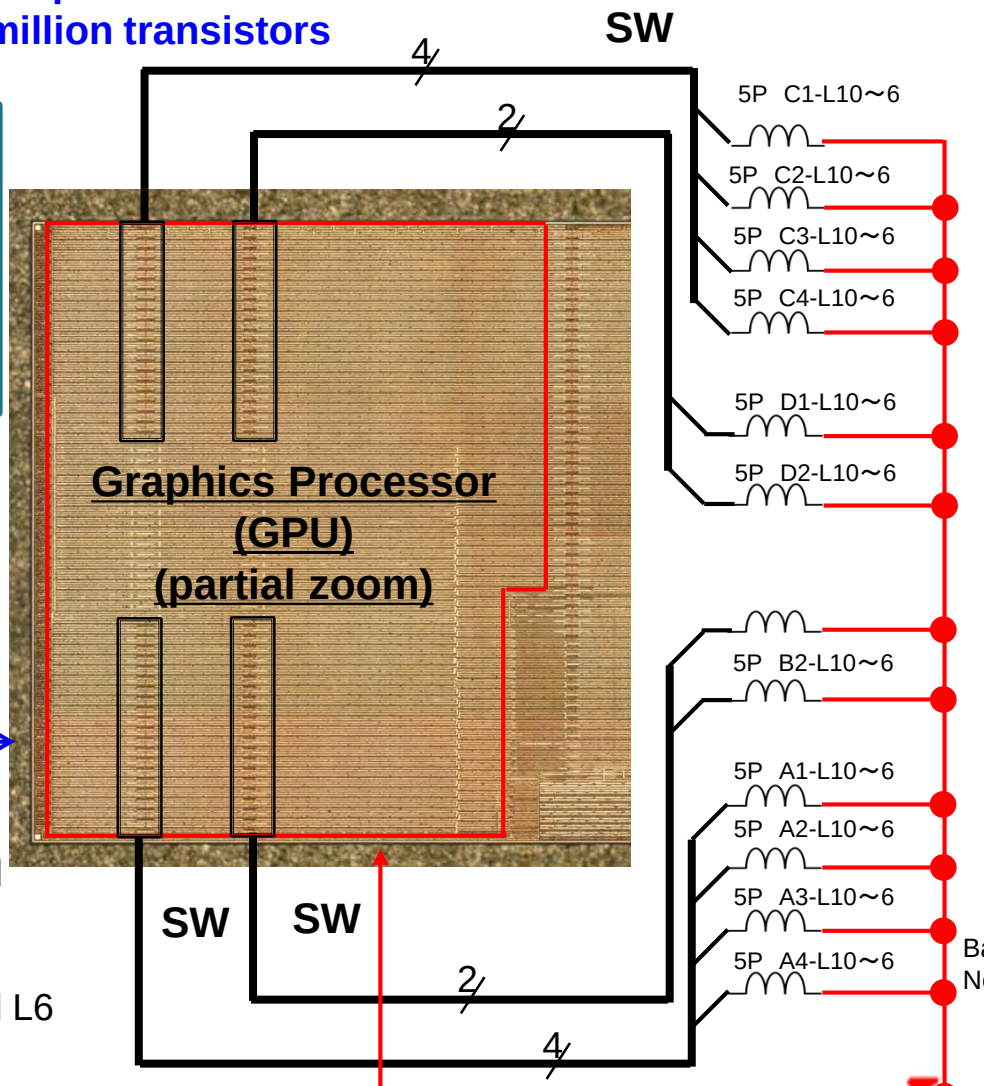
Haswell Granular PwrSoC: Sample Regulator

- **Substrate Layer 10: Six inductors are connected in parallel**
- **12-phase buck converter generates power to the GPU**
- **Each switch is comprised of 3.9 million transistors**



Source Intel Corporation

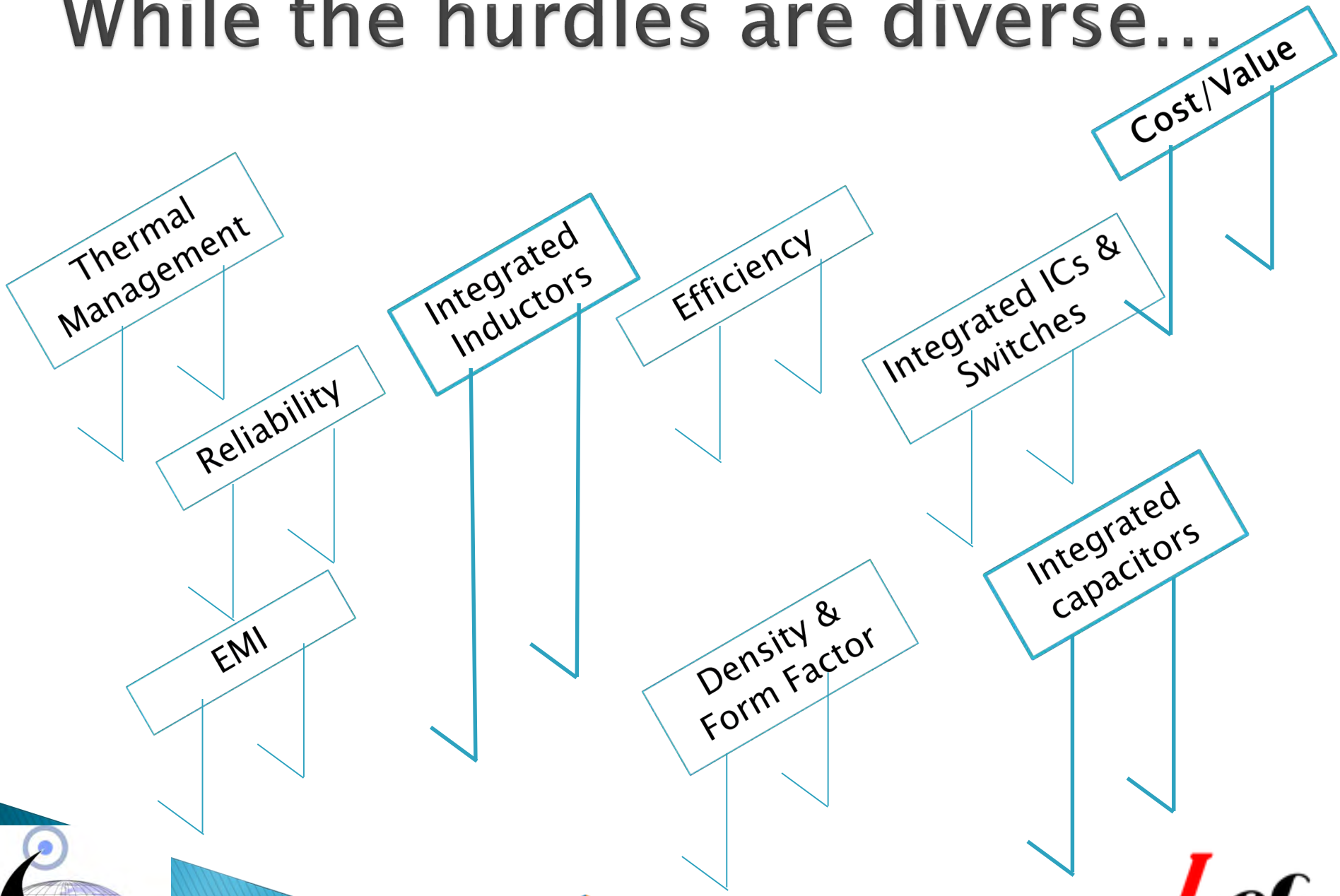




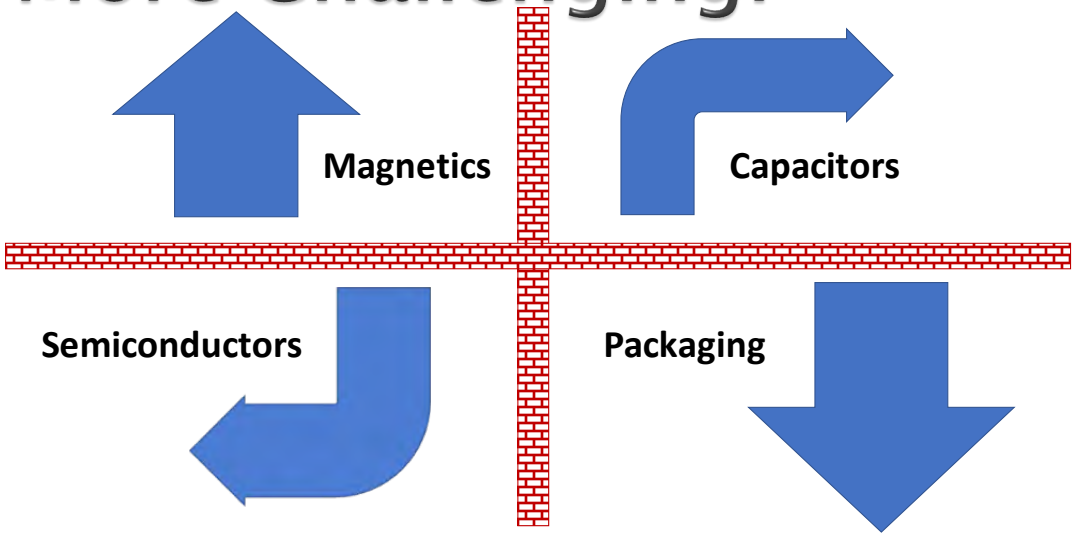
Naming convention: in "5P B2-L10~6"
5P means five inductors parallel connected
B2 is inductor identifier
L10 means Substrate Layer 10
L10-6 means inductors on L10, L9, L7, and L6 are parallel connected

Partial die images. Source LTEC Corporation [2]

While the hurdles are diverse…



…Heterogeneous Business Integration Can Be More Challenging!



- Available internal component sourcing but…Problems confronted
  - Independent business silos – no cooperation and possible internal double margin
  - Conflicting financial incentives
  - Missing silo (e.g. magnetics semiconductor) –requiring external sourcing and again double margins – can be a cost
  - Non optimal designs – external or internal design source limited

In summary

- Integrating semiconductor and power passive components has been a driving focus for most of the past 2 decades.
- Both PSiP and (near) PwrSoC products are a $Billion commercial reality today with the major growth yet to happen.
- Concerted efforts we are seeing at 3D-PEIM is encouraging and I am sure is greatly appreciated by those who have brought us this far.

PWR SOC 18

International Workshop on Power Supply On Chip
October 17-19, 2018
NCTU, Hsinchu, Taiwan

國立交通大學
National Chiao Tung University

Integrated Power Conversion and Power Management

Sessions

- Plenary Session
- Systems & Applications
- Topologies and Control
- Wide-Bandgap Semiconductors and Integration
- Integrated Magnetics
- Integrated Capacitive Devices
- System Integration, Packaging and Manufacturing
- Granular Power Supply

References

1. "Market Report: Power Supply in a Package (PSiP) & Power Supply on a Chip (PwrSoC) –The Power Density Challenge Continues 2015 – 2012," a market report by Anagenesis, Inc., Arnold Alderman and Ada Cheng, published October 2017.
2. Reference: LTEC Brochure: "LEARN ABOUT INTEGRATED POWER MANAGEMENT WITHIN HASWELL PROCESSORS" 14 H076_F https://www.ltecusa.com/haswell
3. "TECHNOLOGY REPORT: Current Developments in 3D Packaging With Focus on Embedded Substrate Technologies PSMA 3D Power Packaging Phase II – A Special Project of the PSMA Packaging Committee," Louis Burgyan, Yuji Kakizaki, Yukata Hama, and Hideki Nakagawa – LTEC Corporation, Arnold Alderman – Anagenesis, Inc., Lars Böettcher & Thomas Löher – Fraunhofer IZM, published by PSMA, March 2015.