SiC Power device structure analysis

Silicon Carbide Semiconductor Device Sample Report

Manufacturer : [redacted]
Package Marking : ----------[redacted]----------
Die Mark : [redacted]----------

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SiC Sample Report List

Makers	Sample situation	Type name	Function
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		SBD
	×		Tr

Makers	Sample situation	Type name	Function
	○		SBD
	×		SBD
	○		SBD
	×		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		SBD
	○		Tr
	○		Tr

LTEC SiC device analysis results

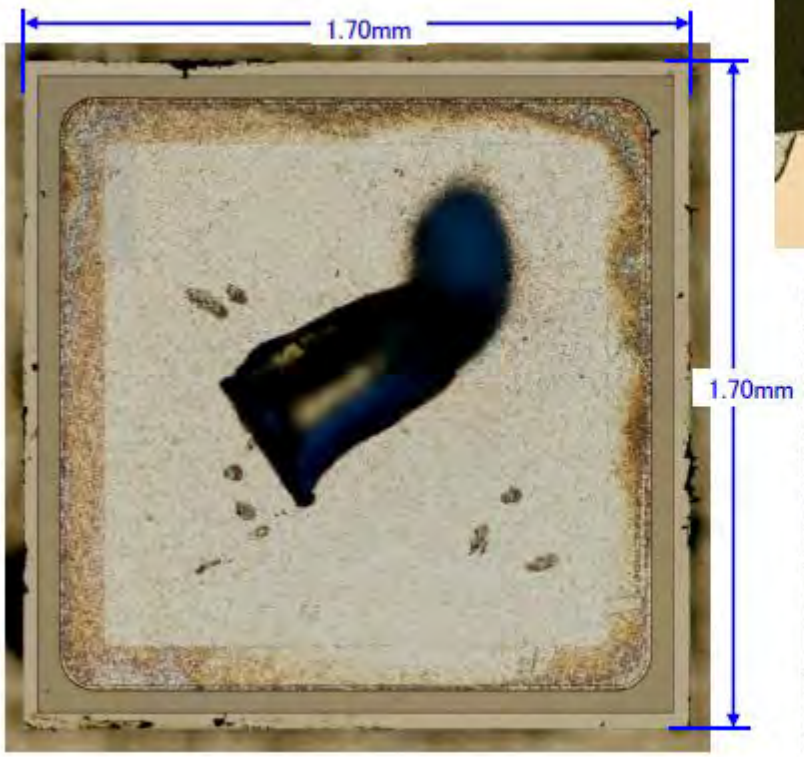
Non JPN 2 companies ; SBD 5 Transistor 1

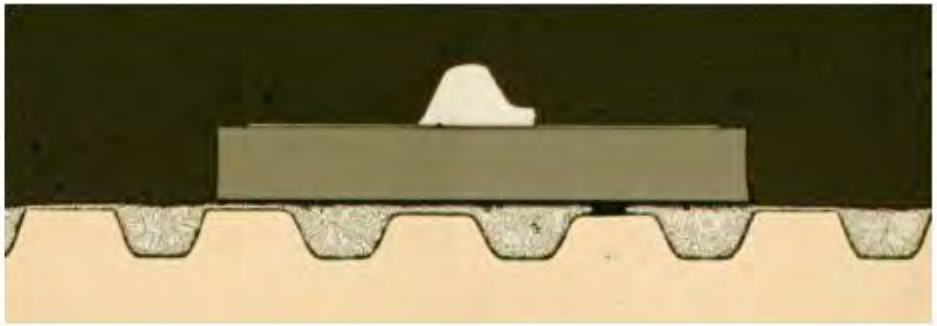
JPN 3 companies ; 4 SBD

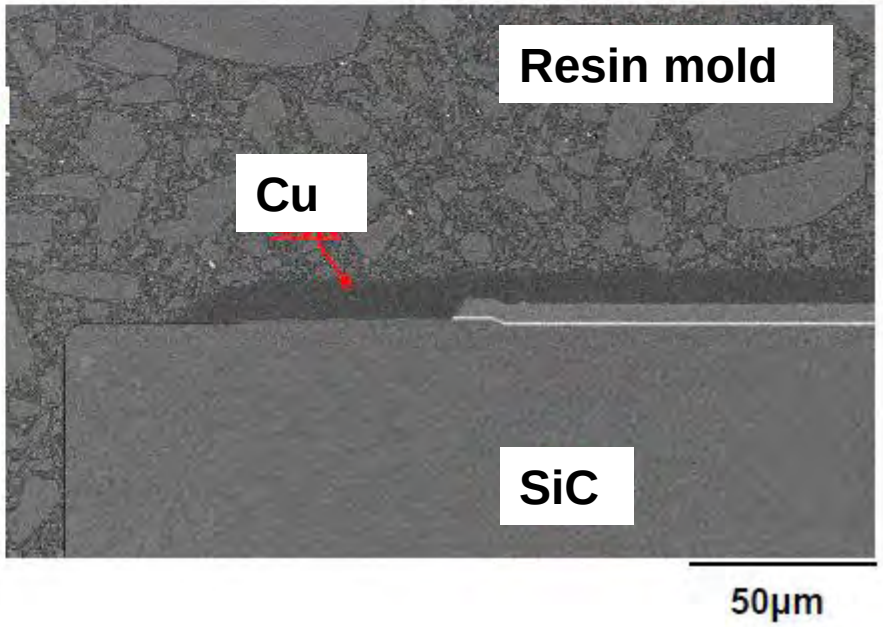
Basic contents of report

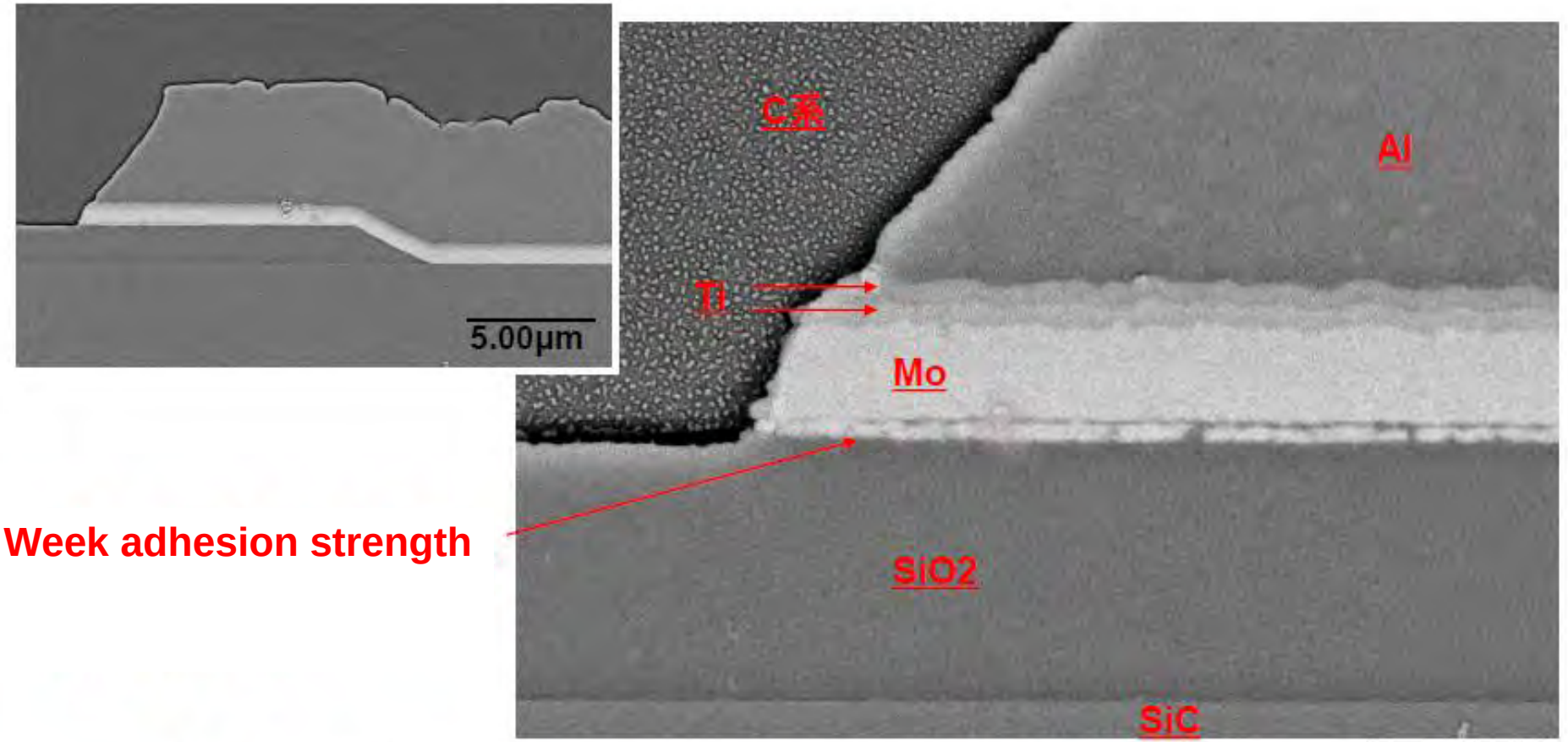
Package outline
Package x-ray image
Package cross section photo
Chip outline
Chip size
Chip (flat layer)
- **Girdling information**
- **Gate wire structure**
- **De-layer**

Chip cross-section (SEM)


1.70mm
1.70mm

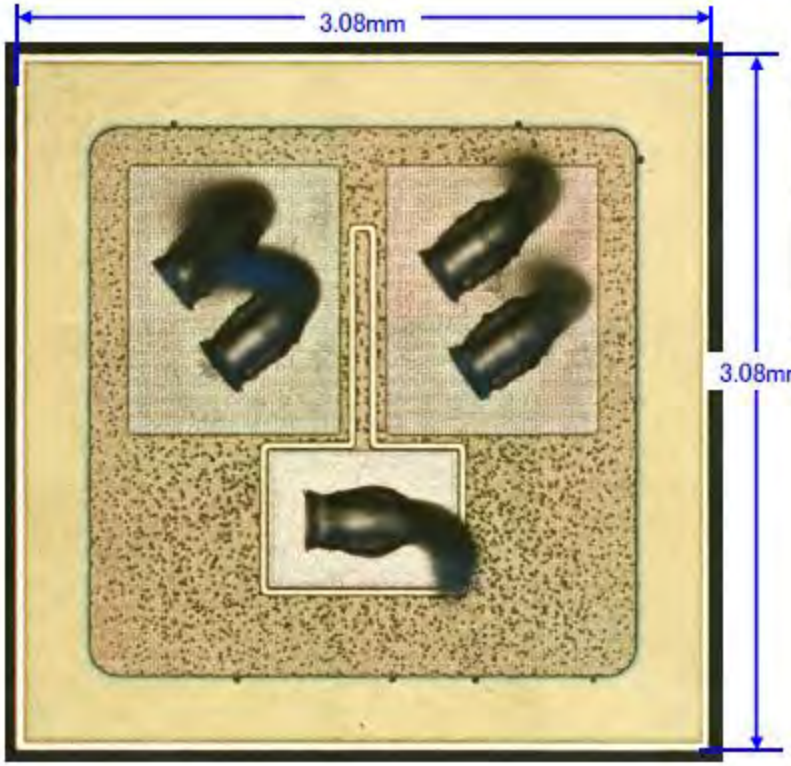


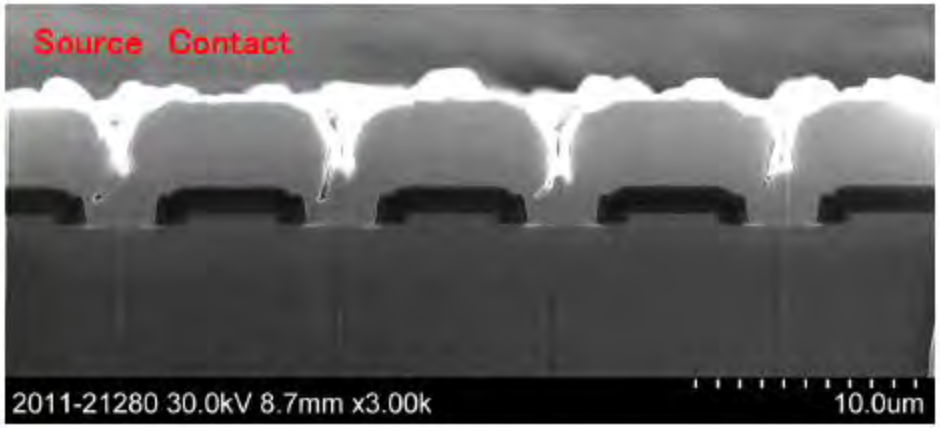

Resin mold
Cu
SiC
50μm

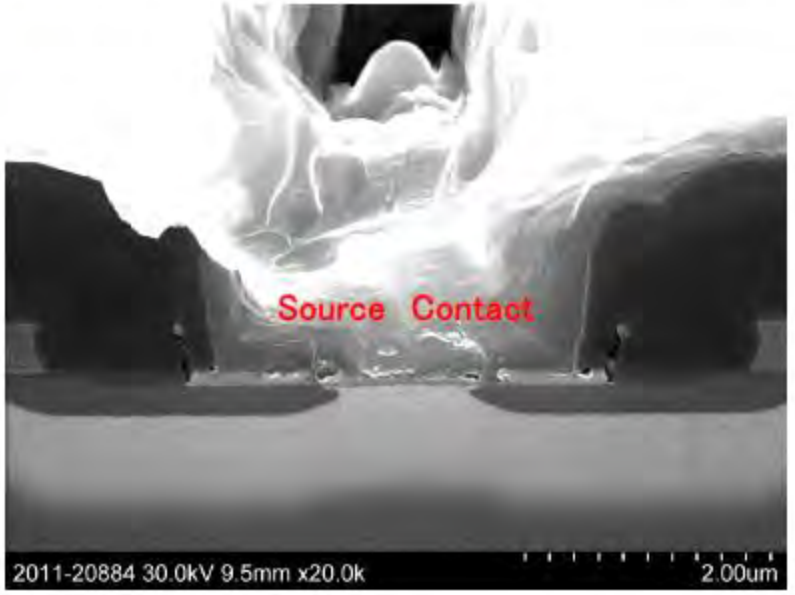


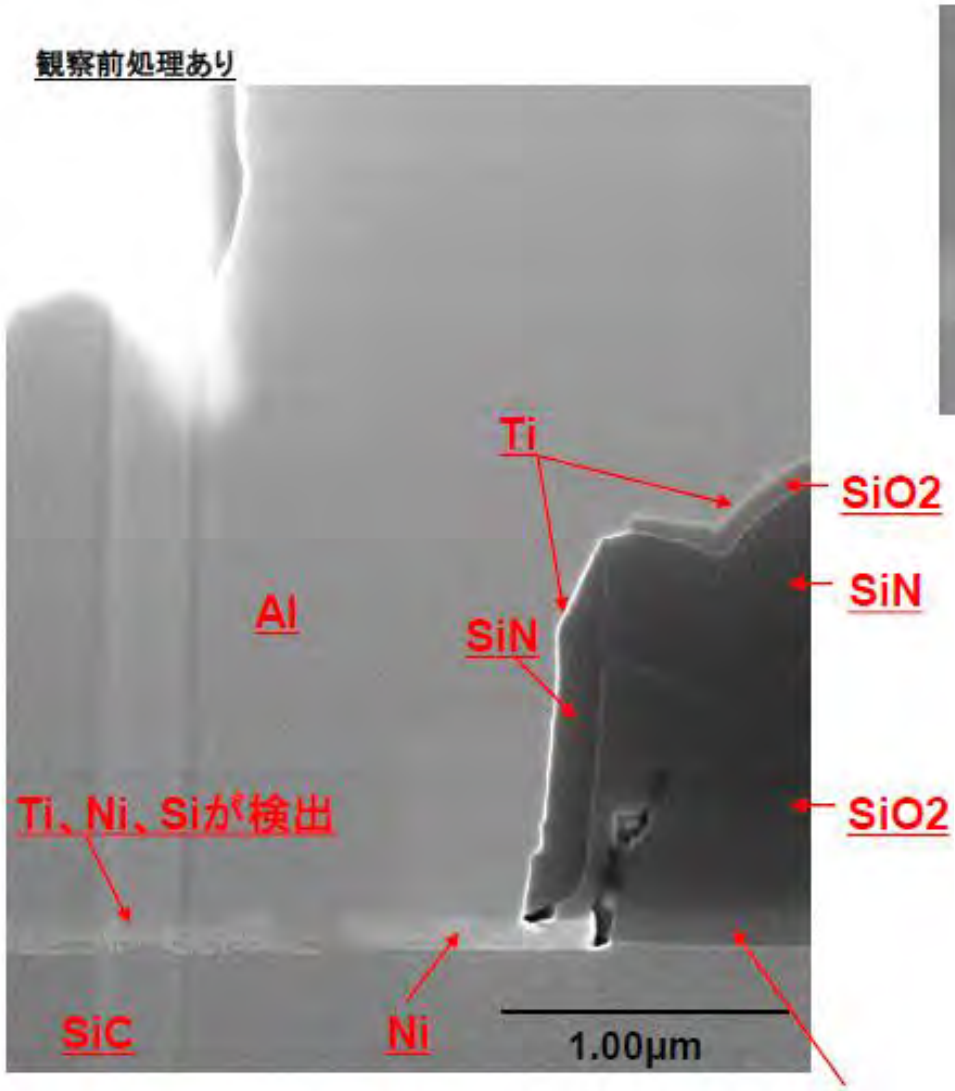
Week adhesion strength

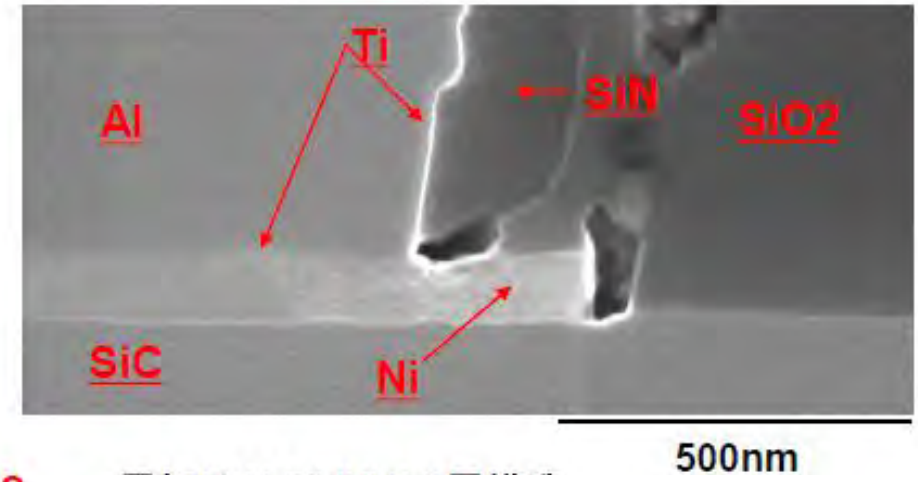
- **4 layer structure electrode Al/Ti/Ti/Mo (Surface of electrode is the organic passivation**
- **Inter layer insulating film is SIO2**


3.08mm
3.08mm


Source Contact
2011-21280 30.0kV 8.7mm x3.00k
10.0um


Source Contact
2011-20884 30.0kV 9.5mm x20.0k
2.00um





- 3 layers electric rode (Al/Ti/Ni)
- Si3N4/SiO2 Inter layer insulating film

1)Form gate insulating film , then contact open
2)Form Ni electric rode by liftoff
3)Form SiO2/SiN film , then contact open
4)Form SW by etch back after growing SiN film
5)Form Al/Ti electric rode

SiO2 gate insulating film