32nm Circuit Analysis Sample Report

(Only selected portions are shown)

DEVICE	Processor
Model Number	xxxxx
Maker	xxxxx
Package Marking	xxxxx
	xxxxx
Chip Marking	xxxxx
Chip Size	;16.0mm × 19.0mm =
Process	304.0mm^2,11Metal-1Poly

IMPORTANT NOTICE
This report, request for investigation, or analysis is intended to assist our client in product development. This report is copyright protected by LTEC Corporation. Our intention is to provide accurate and reliable information to our customer. While we always aim for maximum precision, an absolute accuracy of all contents in this report cannot be guaranteed.
If contents of this report are used in patent infringement disputes, Ltec cannot accept any liability resulting from potential inaccuracies contained in this report.

Contact in the USA:
LTEC Corporation US Representative Office
2280 Zanker Road, No: 203
San Jose CA 95134

Phone: (408) 432-7247
Website: www.ltecusa.com
Contact: info@ltecusa.com

Headquarters:
LTEC Corporation
42-8, 4-chome, Higashiarioka, Itami-city, Hyogo, Japan

Table of Contents

Table1	Chip Information	...	8

Introduction

Photo.1-1	Package (Top View)	...	9
Photo.1-2	Package (Bottom View)	...	9
Photo.2	X-Ray	...	10
Photo.3-1	Chip Overview	...	11
Photo.3-2	Chip Marking	...	11

Elements

Photo.4	MOS Transistor	...	12

Analysis Area

Photo.5-1	Analysis Area (1Metal-Layer)	...	13
Photo.5-2	Analysis Area RAM1 (1Metal-Layer)	...	14
Photo.5-3	Analysis Area RAM2 (1Metal-Layer)	...	15
Photo.5-4	Analysis Area RAM3 (1Metal-Layer)	...	16
Photo.5-5	Analysis Area RAM4 (1Metal-Layer)	...	17
Table2	Function	...	18

Circuit

Fig.1	RAM1 256-Block	...	19
Fig.1-1	RAM1 32-block	...	20
Fig.1-1-1	Master CLK Signal Driver	...	21
Fig.1-1-1-1	Master Control Generation	...	22
Fig.1-1-1-2	Buffer3	...	23
Fig.1-1-2	Buffer1	...	24
Fig.1-1-3	Buffer2	...	25
Fig.1-1-4	RAM1 8-block	...	26
Fig.1-1-4-1	Sense Amp Control1	...	27
Fig.1-1-4-1-1	Control Circuit1	...	28
Fig.1-1-4-1-2	Write Adress Enable2	...	29
Fig.1-1-4-1-3	NAND Circuit	...	30
Fig.1-1-4-1-4	Read Bus Equalize	...	31
Fig.1-1-4-1-4-1	Read Bus Equalize Block	...	32
Fig.1-1-4-1-5	Write Adress Enable1	...	33
Fig.1-1-4-1-6	BL Equalize Block	...	34
Fig.1-1-4-1-6-1	BL Equalize	...	35

Fig.1-1-4-2	Column Decoder and Address Selector	...	36
Fig.1-1-4-2-1	Column Address Decoder and Selector Block	...	37
Fig.1-1-4-2-1-1	Column Address Decoder and Selector	...	38
Fig.1-1-4-3	Row Decoder Block1	...	39
Fig.1-1-4-3-1	Row Block Decoder	...	40
Fig.1-1-4-3-2	Row Address Latch1	...	41
Fig.1-1-4-3-3	Row Address Latch2	...	42
Fig.1-1-4-3-4	Sub WL Driver1	...	43
Fig.1-1-4-3-5	Sub WL Driver2	...	44
Fig.1-1-4-3-6	Row Decoder	...	45
Fig.1-1-4-3-6-1	Row Decoder Cell	...	46
Fig.1-1-4-3-6-1-1	WL Driver Cell	...	47
Fig.1-1-4-4	Memory Cell and Sense Amp1	...	48
Fig.1-1-4-4-1	Memory Cell and Sense Amp Block1	...	49
Fig.1-1-4-4-1-1	Memory Cell and Sense Amp Block Cell1	...	50
Fig.1-1-4-4-1-2	Y-Gate and Sense Amp	...	51
Fig.1-1-4-4-1-2-1	Memory Cell Column	...	52
Fig.1-1-4-4-1-2-1-1	Memory Cell	...	53
Fig.1-1-4-4-1-2-2	Y-Gate	...	54
Fig.1-1-4-4-1-2-3	Sense Amplifier	...	55
Fig.1-1-4-4-2	Memory Cell and Sense Amp Block2	...	56
Fig.1-1-4-4-2-1	Memory Cell and Sense Amp Block Cell2	...	57
Fig.1-1-4-5	RW Bus Shift Block	...	58
Fig.1-1-4-5-1	RW Bus Selector1-1	...	59
Fig.1-1-4-5-1-1	Read Bus Selector Cell	...	60
Fig.1-1-4-5-1-2	Write Bus Selector Cell1	...	61
Fig.1-1-4-5-2	RW Bus Selector1-2	...	62
Fig.1-1-4-5-3	RW Bus Selector1-3	...	63
Fig.1-1-4-5-4	RW Bus Selector1-4	...	64
Fig.1-1-4-5-5	RW Bus Selector1-5	...	65
Fig.1-1-4-5-5-1	Write Bus Selector Cell2	...	66
Fig.1-1-4-6	Sense Amp Control2	...	67
Fig.1-1-4-7	Column Decoder and Address Selector2	...	68
Fig.1-1-4-8	Row Decoder Block2	...	69
Fig.1-1-4-9	Memory Cell and Sense Amp2	...	70
Fig.1-1-4-10	Address Circuit2	...	71
Fig.1-1-4-11	Address Circuit1	...	72
Fig.1-1-4-12	Control Circuit Block	...	73
Fig.1-1-4-12-1	Row Block Select	...	74
Fig.1-1-4-12-2	Column Control2	...	75
Fig.1-1-4-12-3	Column Control2	...	76
Fig.1-1-4-12-4	Column Control1	...	77
Fig.1-1-4-12-5	Column Control3	...	78

Fig.1-1-4-13	Write Bus Control Block	...	79
Fig.1-1-4-13-1	Latch Circuit	...	80
Fig.1-1-4-13-2	Write Address Decoder1	...	81
Fig.1-1-4-13-3	Write Address Decoder2	...	82
Fig.1-2	Read Bus Block x4	...	83
Fig.1-2-1	Read Bus Block	...	84
Fig.1-2-1-1	Read Bus Cell1-1	...	85
Fig.1-2-1-2	Read Bus Cell1-2	...	86
Fig.1-2-1-3	Read Bus Cell2-1	...	87
Fig.1-2-1-4	Read Bus Cell2-2	...	88
Fig.1-3	Write Data Buffer TOP	...	89
Fig.1-3-1	Write Data Buffer Cell 1	...	90
Fig.1-3-1-1	Write Data Buffer	...	91
Fig.1-3-2	Write Data Buffer Cell 2	...	92
Fig.2	RAM2 Block Diagram	...	93
Fig.2-1	Memory Cell Array Block b	...	94
Fig.2-1-1	Memory Cell Array b1	...	95
Fig.2-1-1-1	MC b	...	96
Fig.2-1-2	Memory Cell Array b2	...	97
Fig.2-2	Master Row Block b	...	98
Fig.2-2-1	Row Block b	...	99
Fig.2-2-1-1	Decoded X-Address b Latch1	...	100
Fig.2-2-1-2	Decoded X-Address b Latch2	...	101
Fig.2-2-1-3	X-Decoder and WL Driver b Block1	...	102
Fig.2-2-1-3-1	X-Decoder and WL Driver b cell1	...	103
Fig.2-2-1-3-1-1	WL Driver b cell	...	104
Fig.2-2-1-4	X-Decoder and WL Driver b Block2	...	105
Fig.2-2-1-4-1	X-Decoder and WL Driver b cell2	...	106
Fig.2-3	Read Write Control Block bT	...	107
Fig.2-3-1	Column Block bT	...	108
Fig.2-3-1-1	Column Block Cell1	...	109
Fig.2-3-1-1-1	Write Driver and Sense Amplifier2	...	110
Fig.2-3-1-1-1-1	Write Driver And Sense Amplifier	...	111
Fig.2-3-1-1-1-2	Read Column Selecter and Sense Amplifier	...	112
Fig.2-3-1-1-2	Read Y-Decoder	...	113
Fig.2-3-1-2	Column Block Cell2	...	114
Fig.2-3-1-2-1	Column Block Cell2	...	115
Fig.2-3-1-3	Column Block Cell3	...	116
Fig.2-3-2	Dout Comparator Block bT	...	117
Fig.2-3-2-1	Dout Selector Block0	...	118
Fig.2-3-2-1-1	Dout Selector Cell1	...	119
Fig.2-3-2-1-2	Dout Selector Cell2	...	120
Fig.2-3-2-1-3	Dout Selector Cell3	...	121
Fig.2-3-2-2-1	Dout Selector Cell4	...	123
Fig.2-3-2-3	Comparator Cell0	...	124
Fig.2-3-2-4	Comparator Cell1	...	125

Fig.2-3-3	Dout Comparator Block2 bT	...	126
Fig.2-3-3-1	Dout Selector Block2	...	127
Fig.2-3-3-1-1	Dout Selector Block2-1	...	128
Fig.2-3-3-1-1-1	Dout Selector Cell2-1	...	129
Fig.2-3-3-1-1-2	Dout Selector Cell2-2	...	130
Fig.2-3-3-1-2	Dout Selector Block2-2	...	131
Fig.2-3-3-1-3	Dout Selector Block2-3	...	132
Fig.2-3-3-1-4	Dout Selector Block2-4	...	133
Fig.2-3-3-2	Dout Comparator2	...	134
Fig.2-3-3-2-1	Dout Comparator Cell2-1	...	135
Fig.2-3-3-2-1-1	XNOR XOR Cell1	...	136
Fig.2-3-3-2-1-2	andnor1	...	137
Fig.2-3-3-2-1-3	andnor2	...	138
Fig.2-3-3-2-2	Dout Comparator Cell2-2	...	139
Fig.2-3-3-2-3	Dout Comparator Cell3	...	140
Fig.2-3-3-2-4	andnor3	...	141
Fig.2-3-4	Dout Selector Block b3 T	...	142
Fig.2-3-4-1	Dout Selector cell b3	...	143
Fig.2-4	Read Write Control Block bB	...	144
Fig.2-4-1	Column Block bB	...	145
Fig.2-4-2	Dout Comparator Block bB	...	146
Fig.2-4-2-1	Dout Selector Block3	...	147
Fig.2-4-2-2	Dout Selector Block4	...	148
Fig.2-4-2-3	Comparator Cell2	...	149
Fig.2-4-2-4	Comparator Cell3	...	150
Fig.2-4-3	Dout Comparator Block3 bB	...	151
Fig.2-4-3-1	Dout Selector Block3b	...	152
Fig.2-4-3-1-1	Dout Selector Block3-1	...	153
Fig.2-4-3-1-2	Dout Selector Block3-2	...	154
Fig.2-4-3-1-3	Dout Selector Block3-3	...	155
Fig.2-4-3-1-4	Dout Selector Block3-4	...	156
Fig.2-4-3-2	Dout Comparator3b	...	157
Fig.2-4-4	Dout Selector Block b3 B	...	158
Fig.2-5	Read Write Control Block bL	...	159
Fig.2-5-1	Read Write Clock bL	...	160
Fig.2-5-1-1	Variable Delay b2	...	161
Fig.2-5-2	Read Y-Gate Control bL	...	162
Fig.2-5-3	Read Control bL	...	163
Fig.2-5-3-1	Variable Delay b1	...	164
Fig.2-5-4	Write Y-Decoder bL	...	165
Fig.2-5-4-1	Write Y-Decoder bL Cell1	...	166
Fig.2-5-4-2	Write Y-Decoder bL Cell2	...	167

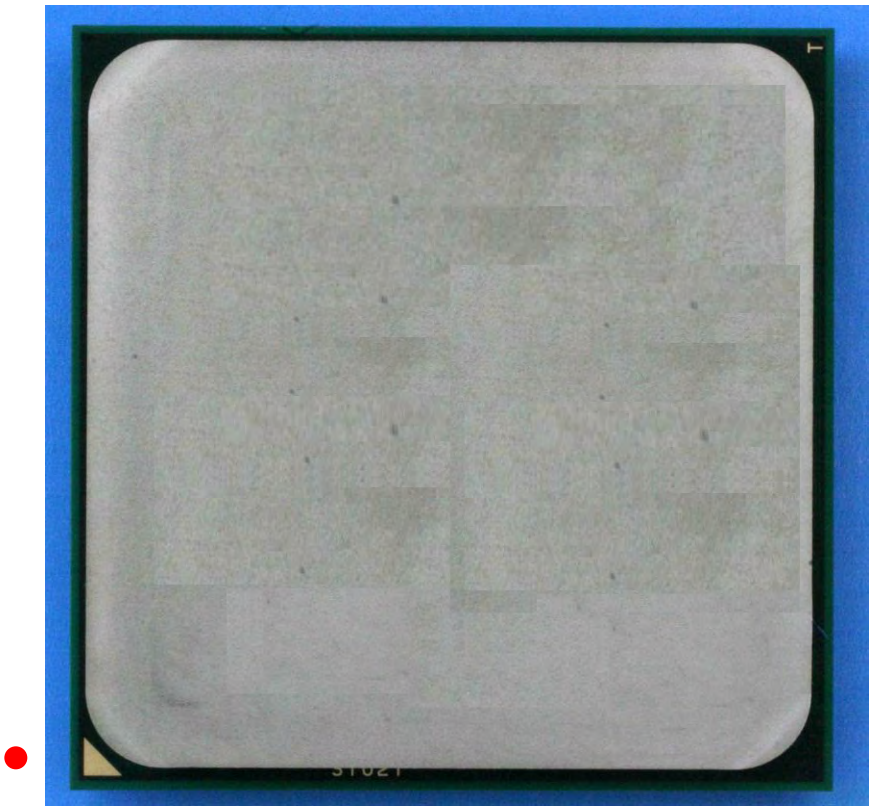
Fig.2-6	Read Write Control Block bR	...	168
Fig.2-6-1	Read Write Clock bR	...	169
Fig.2-6-2	Read Y-Gate Control bR	...	170
Fig.2-6-3	Read Control bR	...	171
Fig.2-6-4	Write Y-Decoder bR	...	172
Fig.2-6-4-1	Write Y-Decoder bR Cell1	...	173
Fig.2-6-4-2	Write Y-Decoder bR Cell2	...	174
Fig.2-7	Dout Comparator Block3	...	175
Fig.2-7-1	Read Clock b	...	176
Fig.2-7-2	Read Decoder b	...	177
Fig.2-7-3	Decoded Y-Address Clock b	...	178
Fig.2-7-3-1	Buffer 6s	...	179
Fig.2-7-4	2nd Dout Comparator2 b	...	180
Fig.2-7-5	B-7	...	181
Fig.2-7-6	Comparated Dout selector b	...	182
Fig.2-7-7	2nd Dout Comparator 1-2b	...	183
Fig.2-8	Write Data Block	...	184
Fig.2-8-1	Write Data Drive sub-block b 1-1	...	185
Fig.2-8-1-1	Write Data Drive sub-block b 1-1-1	...	186
Fig.2-8-1-1-1	Write Data Drive sub-block b 1-1-1	...	187
Fig.2-8-1-2	Write Data Drive sub-block b 1-1-2	...	188
Fig.2-8-1-3	Write Data Drive sub-block b 1-1-3	...	189
Fig.2-8-2	Write Data Drive Block b 2-1	...	190
Fig.2-8-2-1	Latch	...	191
Fig.2-8-3	Data Address Decoder b1	...	192
Fig.2-8-4	Data Address Decoder b2	...	193
Fig.2-8-5	Write Data Drive sub-block b 1-2	...	194
Fig.2-8-5-1	Write Data Drive sub-block b 1-2-1	...	195
Fig.2-8-5-2	Write Data Drive sub-block b 1-2-2	...	196
Fig.2-8-5-2-1	Write Data Drive cell b 1-2	...	197
Fig.2-8-5-3	Write Data Drive sub-block b 1-2-3	...	198
Fig.2-8-6	Write Data Drive Block b 2-2	...	199
Fig.2-8-7	Write Control Clock b	...	200
Fig.2-8-8	Clock Generator for Decoder	...	201
Fig.3	RAM3 Block Diagram	...	202
Fig.3-1	Read Write Block	...	203
Fig.3-1-1	Write Driver	...	204
Fig.3-1-2	Not Used Write Driver	...	205
Fig.3-1-3	Read Out Block1	...	206
Fig.3-1-3-1	Memory Array1	...	207
Fig.3-1-3-1-1	Memory Array Cell	...	208
Fig.3-1-3-2	Memory Array2	...	209
Fig.3-1-3-3	Read Circuit	...	210
Fig.3-1-4	Read Out Circuit	...	211
Fig.3-1-5	Not Used Read Out Circuit	...	212

Fig.3-2	Read Switch Controller	...	213
Fig.3-2-1	Read Switch Control	...	214
Fig.3-3	Gate Switch Controller	...	215
Fig.3-3-1	Gate Switch Control	...	216
Fig.3-4-1	Read X Add Buf1	...	217
Fig.3-4-2	Read Y Add Buf1	...	218
Fig.3-4-3	Gate X Add Buf1	...	219
Fig.3-4-4	Gate Y Add Buf1	...	220
Fig.3-4-5	Read X Add Buf2	...	221
Fig.3-4-6	Read Y Add Buf2	...	222
Fig.3-4-7	Gate X Add Buf2	...	223
Fig.3-4-8	Gate Y Add Buf2	...	224
Fig.3-5	Add Delay	...	225
Fig.3-5-1	Add Delay Cell	...	226
Fig.3-6	Block Selector1	...	227
Fig.3-7	Write Gate Latch Switch Controller	...	228
Fig.3-8	Block Selector2	...	229
Fig.3-9	Block Selector3	...	230
Fig.3-10	Logic	...	231
Fig.3-11-1	Timing Controller1	...	232
Fig.3-11-2	Timing Controller2	...	233
Fig.4-1	Dout Shift Signal Generator Block d	...	234
Fig.4-1-1	Dout Shift Address Clock d	...	235
Fig.4-1-2	Dout Shift Address Buffer d cell	...	236
Fig.4-1-3	Dout Shift Address Decoder d-Cell-1	...	237
Fig.4-1-4	Dout Shift Address Decoder d Cell-2	...	238
Fig.4-2	Dout Din Block d	...	239
Fig.4-2-1	Dout Din Sub Block d 1R	...	240
Fig.4-2-1-1	Dout Circuit and Write Driver Block d	...	241
Fig.4-2-1-1-1	1 BYTE Memory Cell d	...	242
Fig.4-2-1-1-1-1	Memory cell d	...	243
Fig.4-2-1-2	Write Circuit d	...	244
Fig.4-2-1-3	Write Driver d	...	245
Fig.4-2-1-4	BL Precharge d	...	246
Fig.4-2-1-5	Read Circuit d	...	247
Fig.4-2-1-6	Dout Circuit d	...	248
Fig.4-2-2	Dout Din Sub Block d 2R	...	249
Fig.4-2-3	Dout Din Sub Block d 3R	...	250
Fig.4-2-4	Dout Din Sub Block d 4R	...	251
Fig.4-2-5	Dout Din Sub Block d 1L	...	252
Fig.4-2-6	Dout Din Sub Block d 2L	...	253
Fig.4-2-7	Dout Din Sub Block d 3L	...	254
Fig.4-2-8	Dout Din Sub Block d 4L	...	255
	Logic cell	...	256

Table1 Chip Information

DEVICE	Processor
Model Number	xxxxxx
Maker	AMD
Package Type	940-pin micro-PGA
Package Marking	xxxxxxx 2011
Chip Marking	xxxxxxx
Chip Size	16.0mm X 19.0mm = 304mm^2
Process	11Metal-1Poly
Process Type	SOI
Gate Length	32nm

Introduction



1Pin

Photo.1-1 Package (Top View)

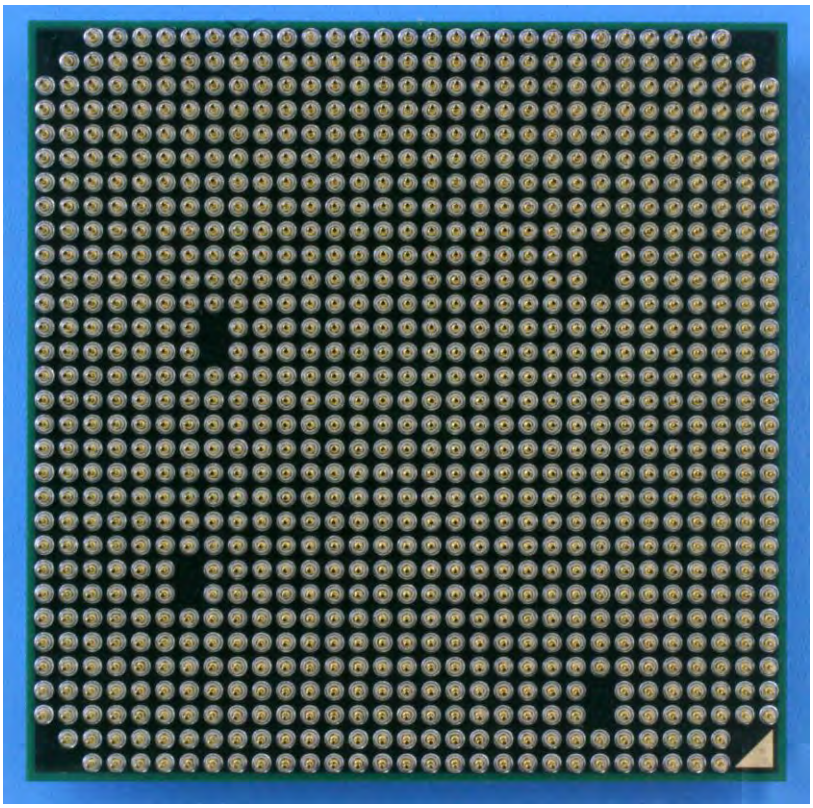
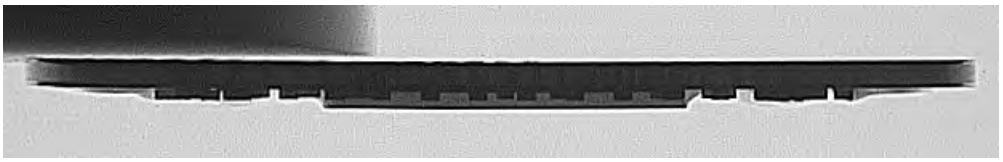
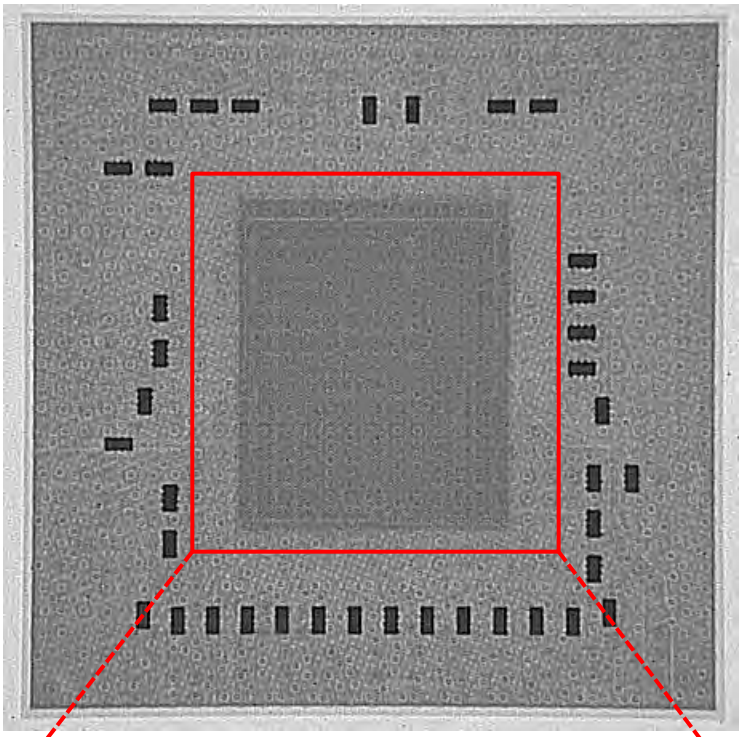


Photo.1-2 Package (Bottom View)



（Side View）

Side View



1Pin

（Top View）

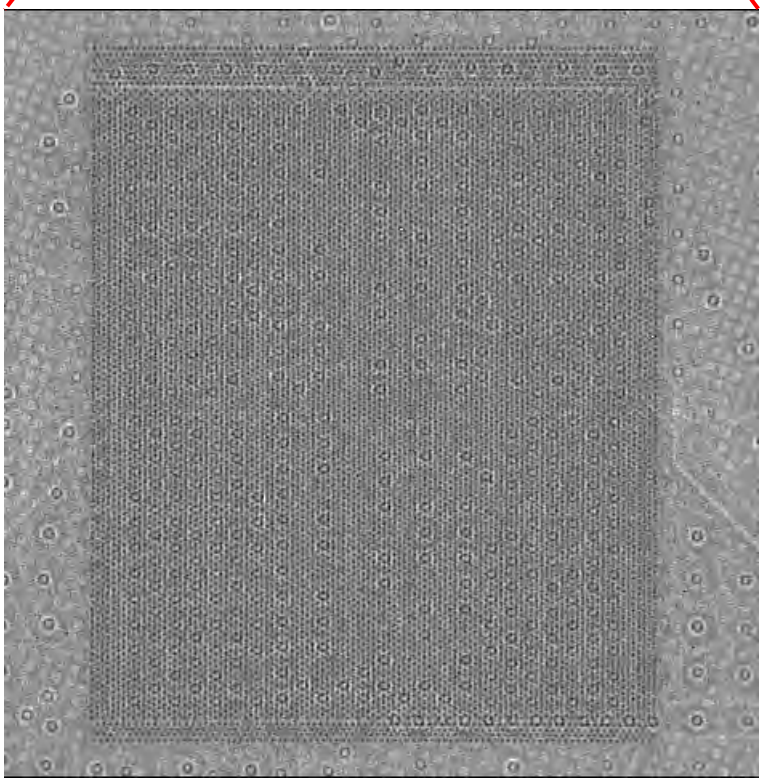


Photo.2 X-Ray

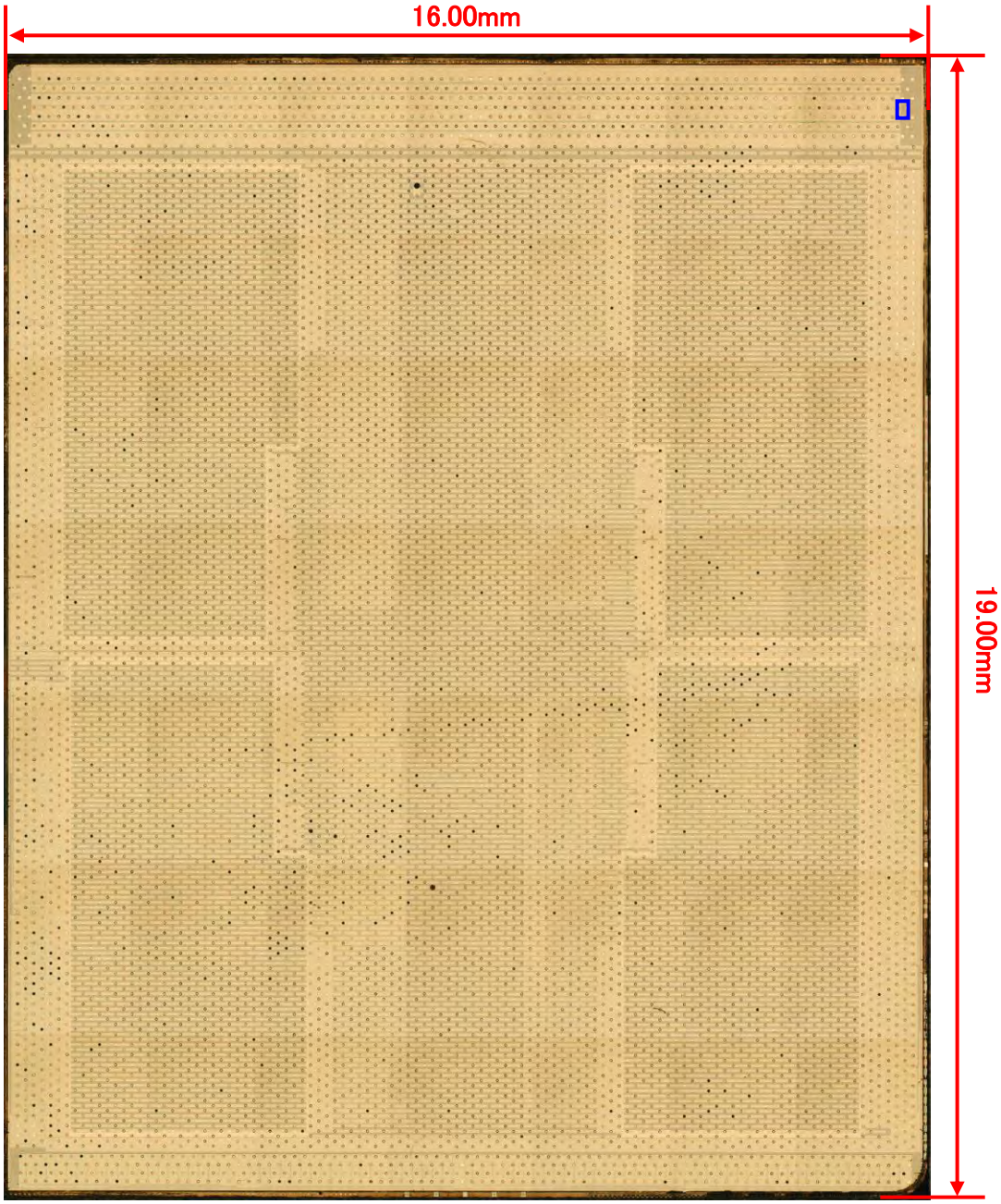


Photo.3-1 Chip Overview

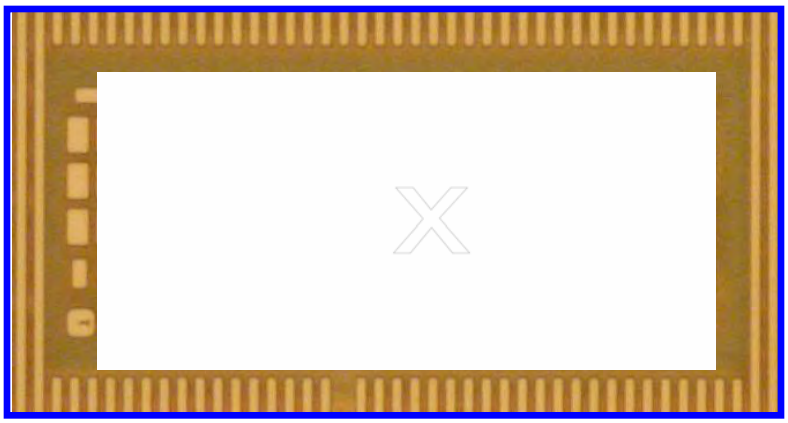
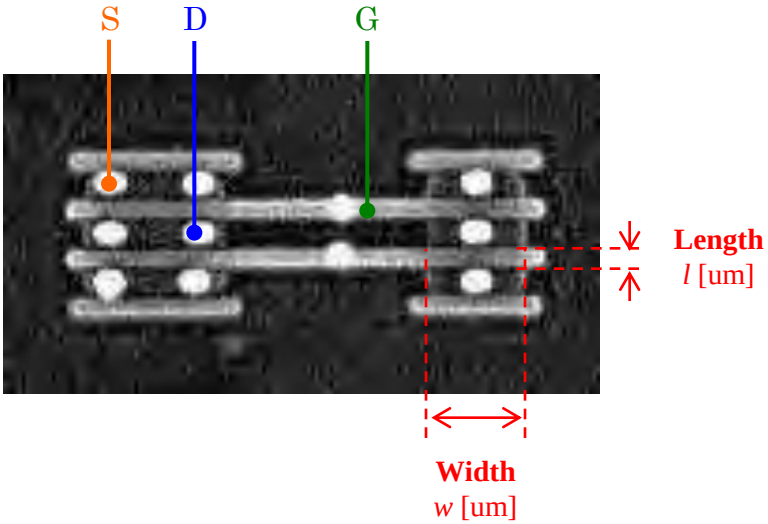
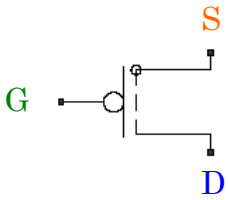
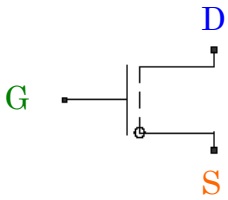


Photo.3-2 Chip Marking

Elements

Layout



	Cell Name	Symbol
[PMOS]	mfetp3-1	 Mn W=*w* u L=*l* u M=*m* mfetp3-1
[NMOS]	mfetn3-1	 Mn W=*w* u L=*l* u M=*m* mfetn3-1

n : element number
m : multiplier

Photo.4 MOS Transistor

Analysis Area

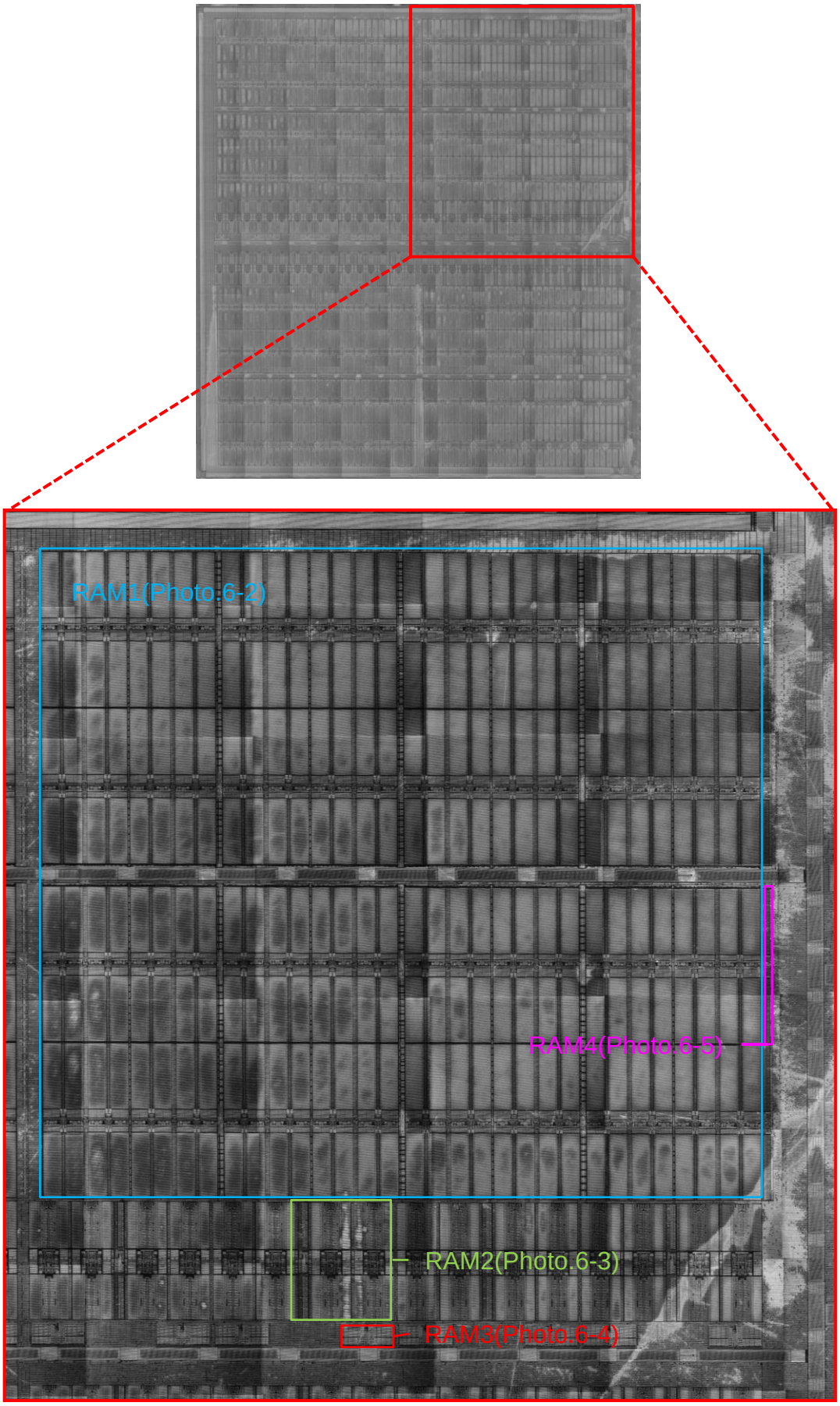
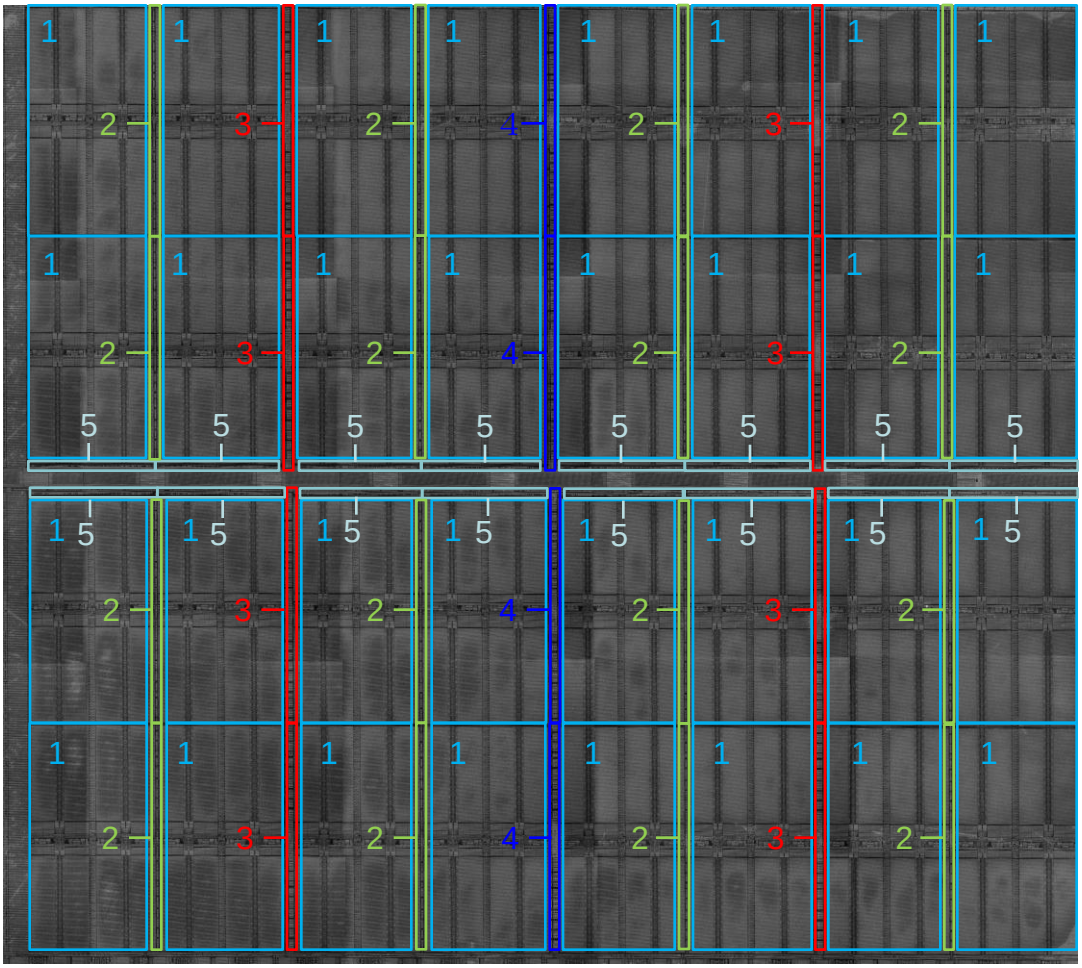


Photo.6-1 Analysis Area (1Metal-Layer)



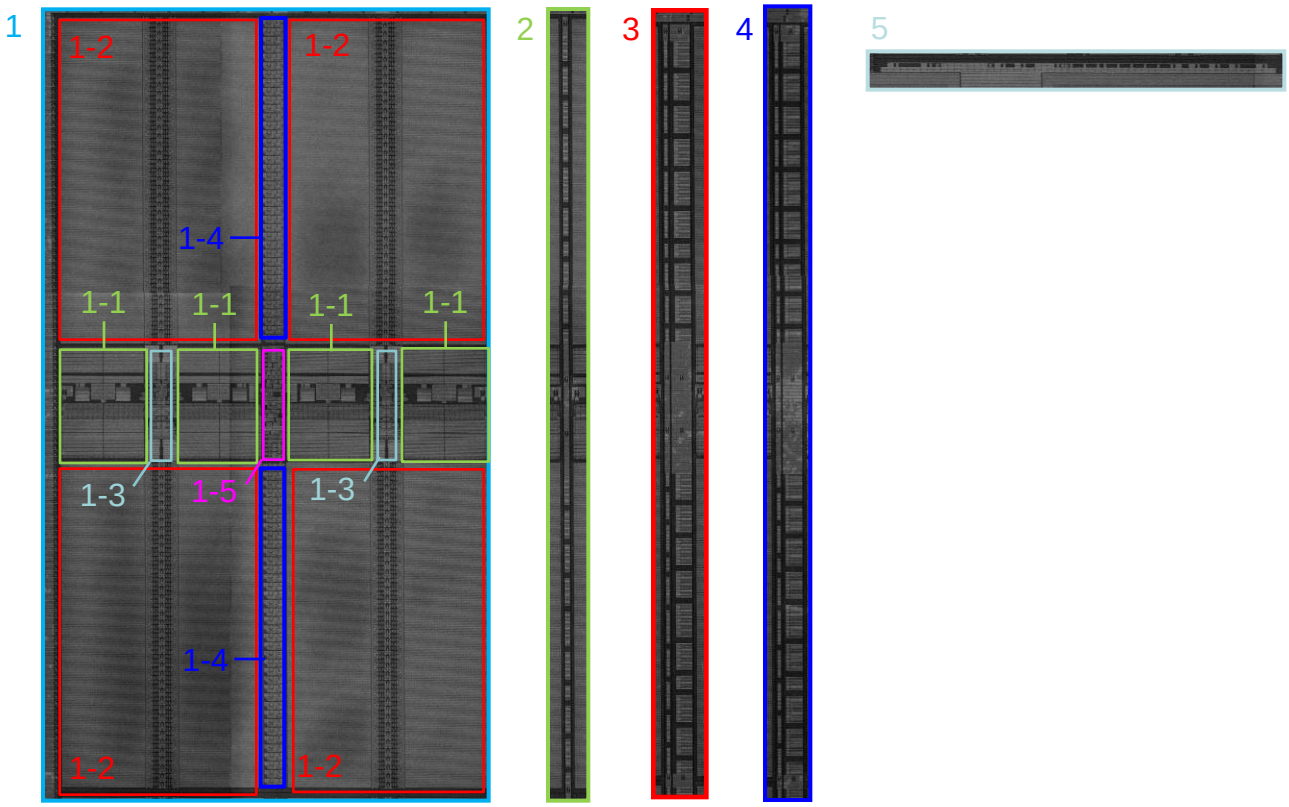


Photo.6-2 Analysis Area RAM1 (1Metal-Layer)

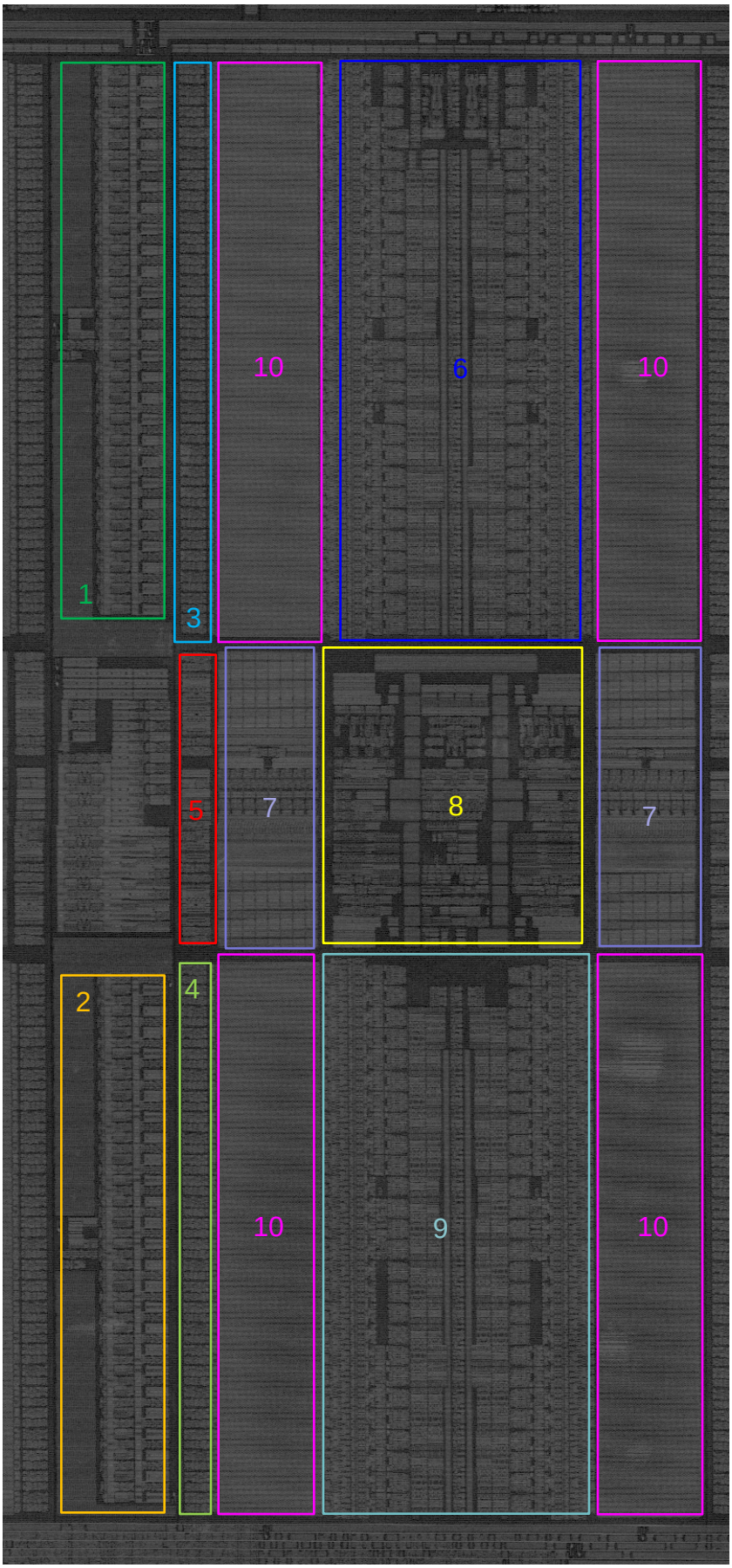
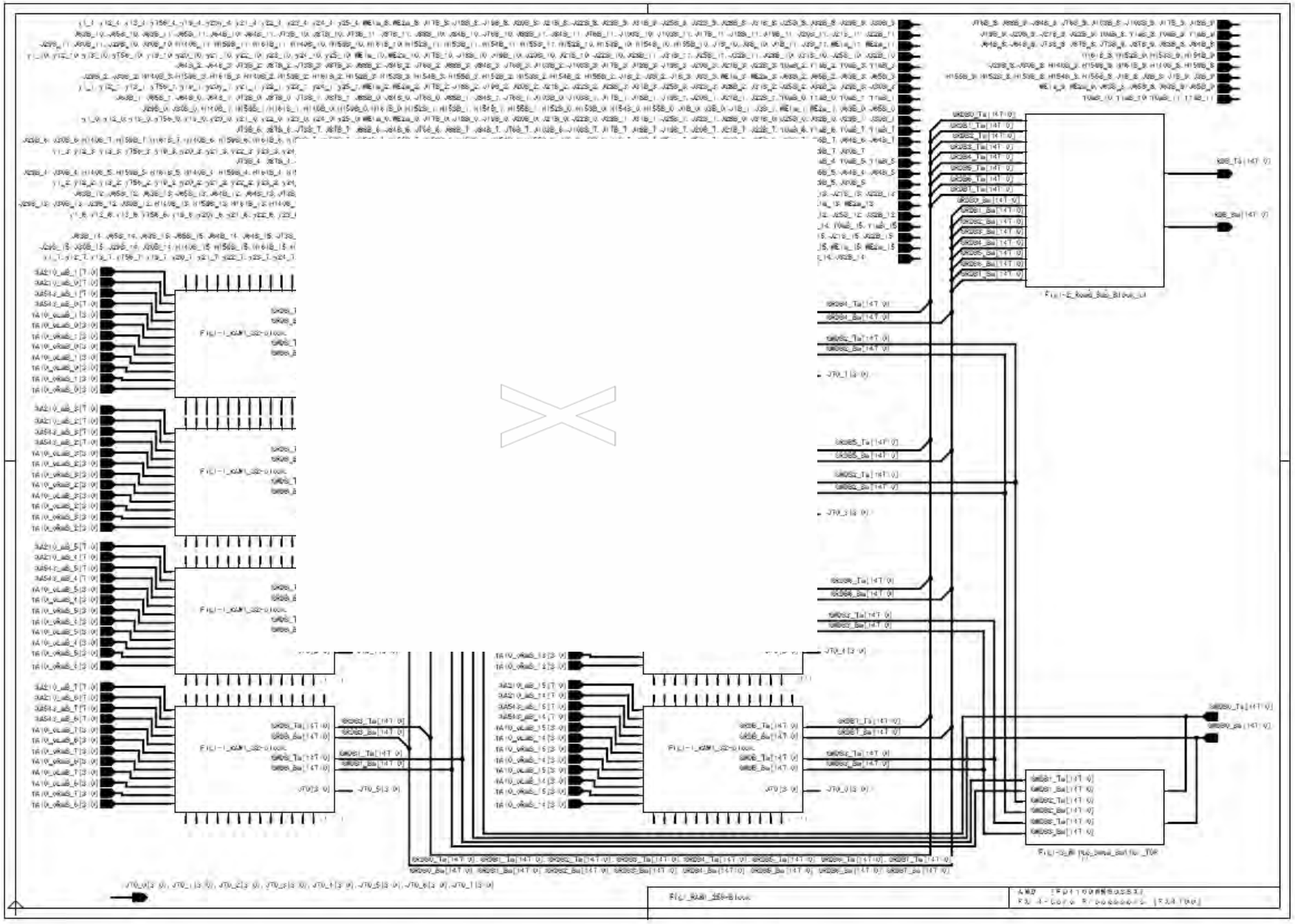


Photo.6-3 Analysis Area RAM2 (1Metal-Layer)

Table2 Function

Function Block		Fig.No	Circuit Name
RAM1		Fig.1	RAM1_256-Block
	Area1-1	Fig.1-1	RAM1_32-block
	Area1-2		
	Area1-3		
	Area1-4		
	Area1-5		
	Area2 Area3 Area4	Fig.1-2	Write_Data_Buffer_Block Read_Bus_Block
	Area5	Fig.1-3	Buffer1 Buffer2 Buffer3
RAM2		Fig.2	RAM2_Block_Diagram
	Area1	Fig.2-8	Write_Data_Block
	Area2		
	Area3		
	Area4		
	Area5		
	Area6	Fig.2-3	Read_Write_Control_Block_bT
	Area7	Fig.2-2	Master_Row_Block_b
	Area8	Fig.2-5 Fig.2-6 Fig.2-7	Read_Write_Control_Block_bL Read_Write_Control_Block_bR Dout_Comparator_Block3
	Area9	Fig.2-4	Read_Write_Control_Block_bB
	Area10	Fig.2-1	Memory_cell_Array_Block_b
RAM3		Fig.3	RAM3_Block_Diagram
	Area1	Fig.3-1	Read_Write_Block
	Area2	Fig.3-7	Write_Gate_Latch_SW_Controller
	Area3	Fig.3-5 Fig.3-6 Fig.3-8 Fig.3-9 Fig.3-10 Fig.3-11	Add_Delay Block_Selector1 Block_Selector2 Block_Selector3 Logic Timing_Controller
	Area4	Fig.3-2 Fig.3-3	Read_SW_Controller Gate_SW_Controller
	Area5	Fig.3-4	Read_Y_Add_Buf1 Gate_Y_Add_Buf1
	Area6		Read_X_Add_Buf1 Gate_X_Add_Buf1 Block_Selector3
	Area7		Read_X_Add_Buf2 Gate_X_Add_Buf2 Block_Selector2
	Area8		Read_Y_Add_Buf2 Gate_Y_Add_Buf2
RAM4		Fig.4	-
	Area1	Fig.4-1	Dout_Shift_Signal_Generator_Block_d
	Area2	Fig.4-2	Dout_Din_Block_d



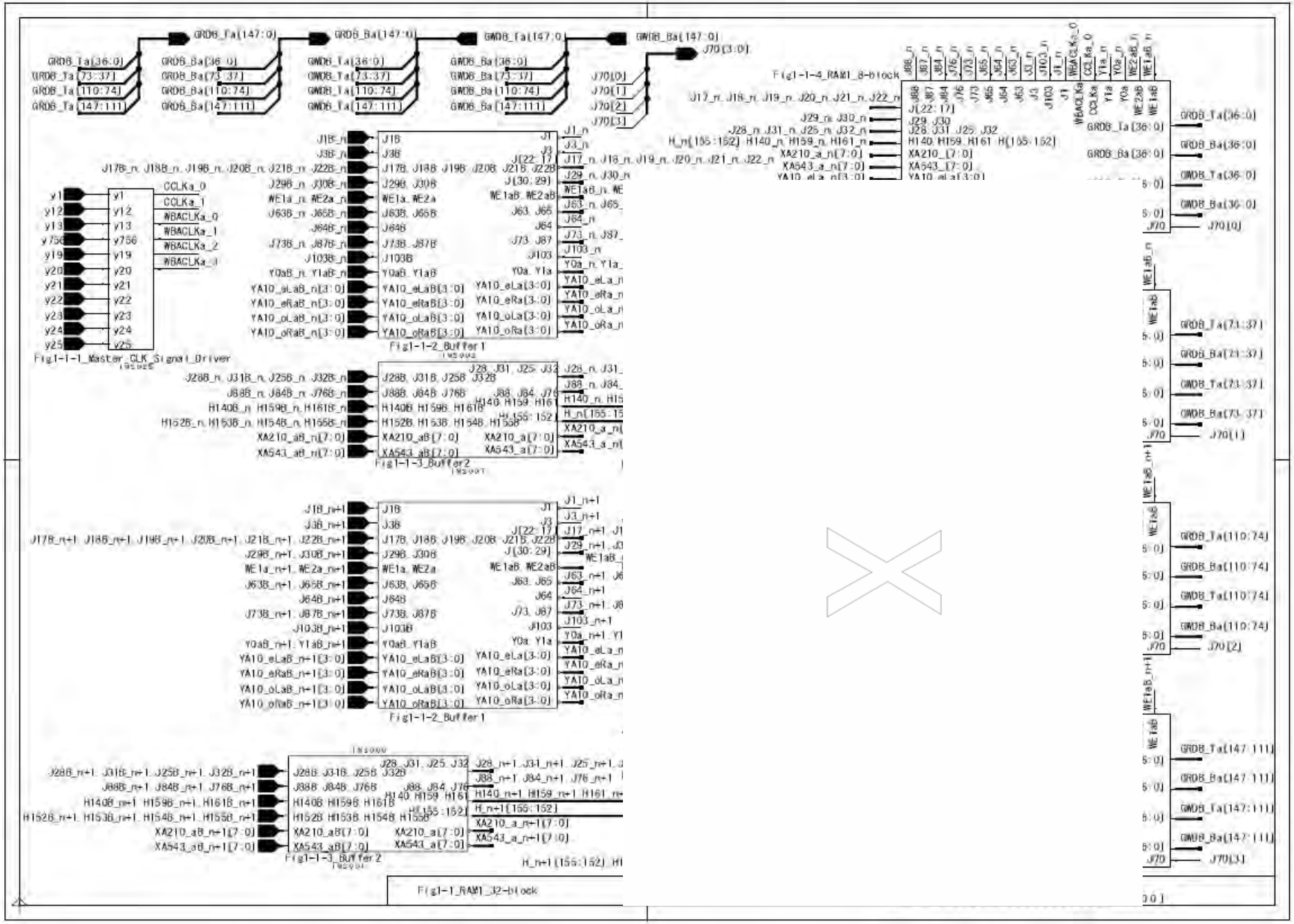
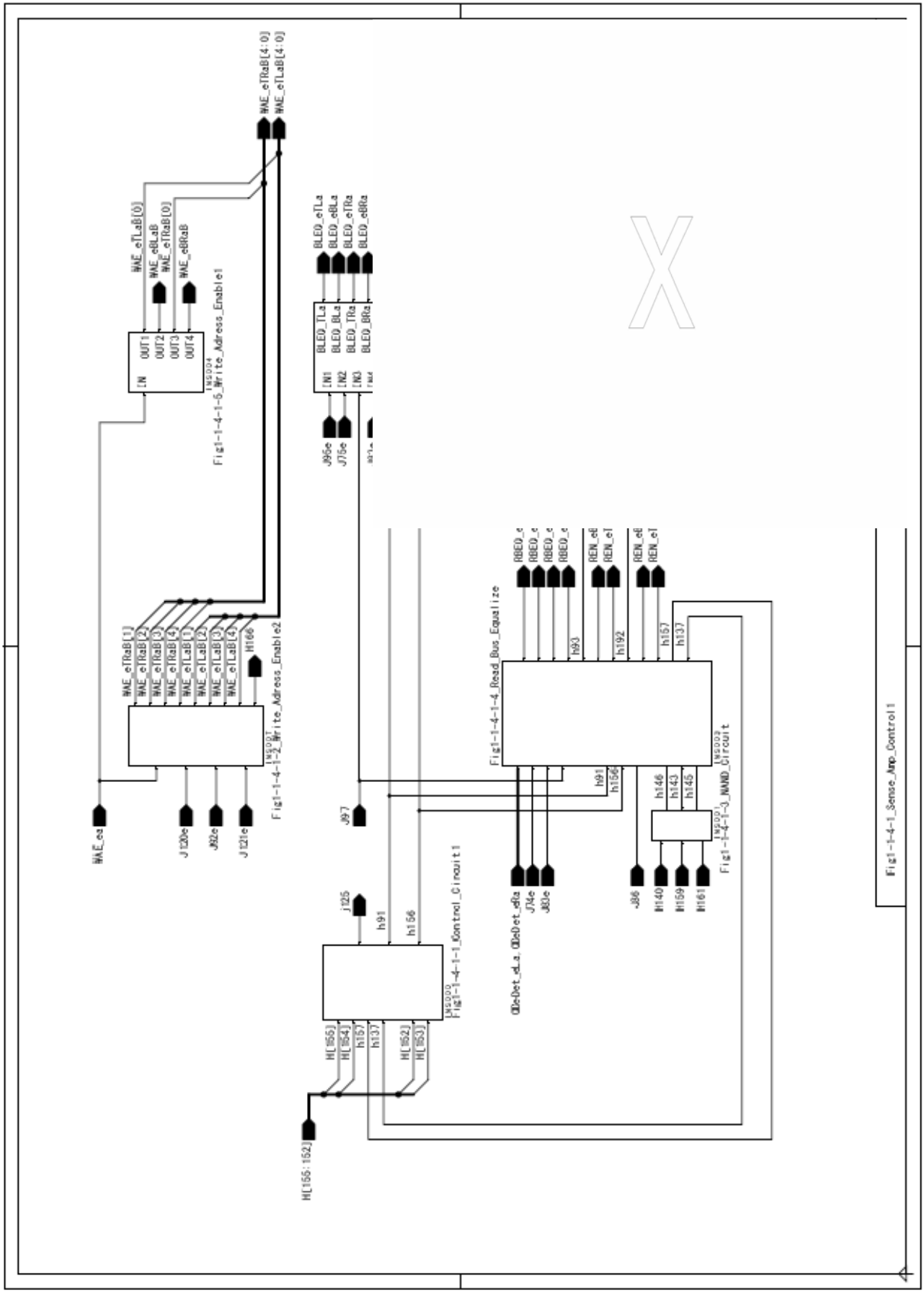
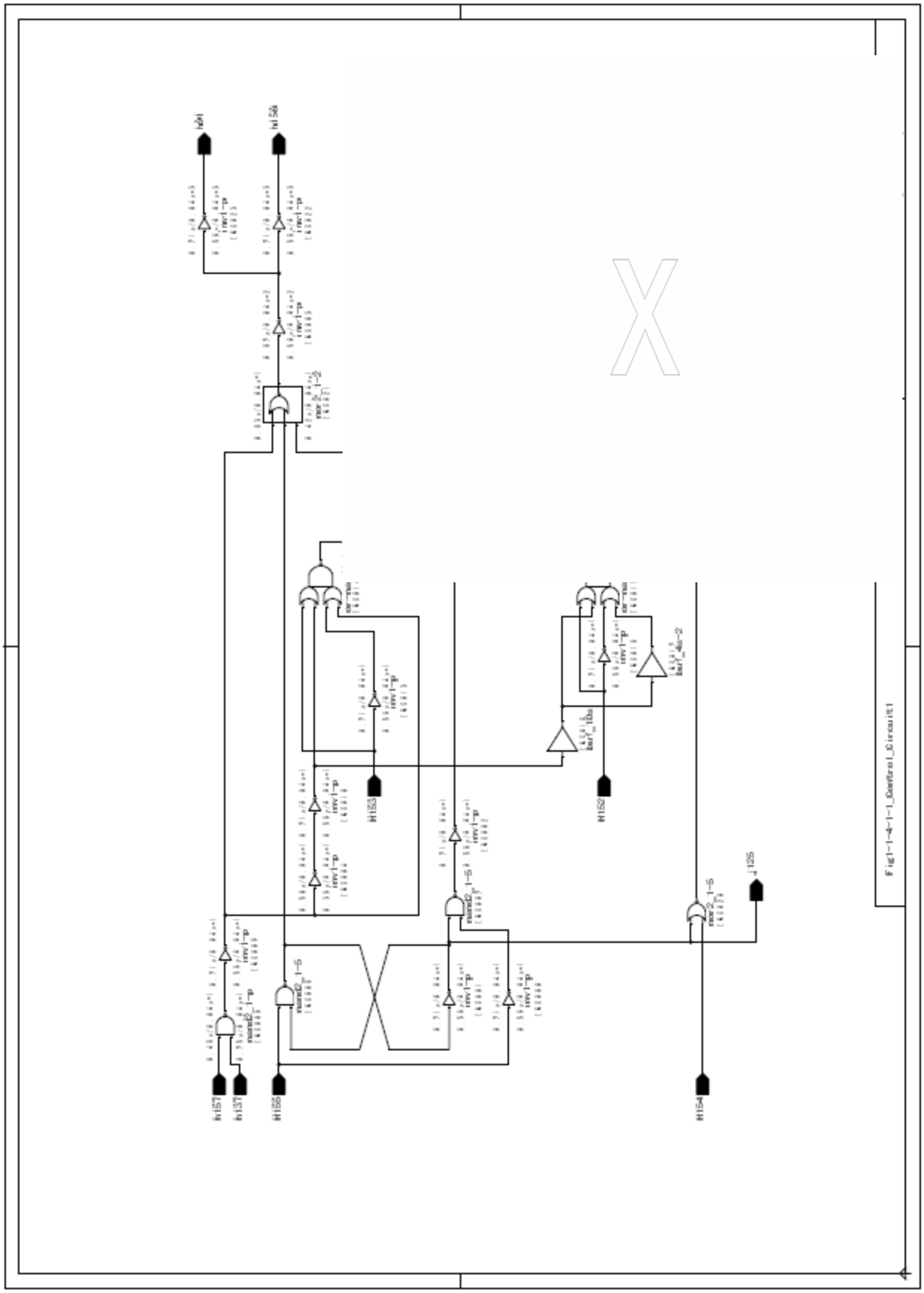


Fig1-1-1_Master_CLK_Signal_Driver
Fig1-1-2_Buffer1
Fig1-1-3_Buffer2
Fig1-1-4_RAM1_8-block
Fig1-1_RAM1_32-block


WAE_eTRaB[4:0]
WAE_eTLaB[4:0]
WAE_eTLaB[0]
WAE_eBLaB
WAE_eTRaB[0]
WAE_eBRaB
IN
OUT1
OUT2
OUT3
OUT4
INS004
Fig1-1-4-1-5_Write_Adress_Enable1
BLED_eTLa
BLED_eBLa
BLED_eTRa
BLED_eBRa
BLED_TLa
BLED_BLa
BLED_TRa
BLED_BRa
IN1
IN2
IN3
J95e
J75e
WAE_eTRaB[1]
WAE_eTRaB[2]
WAE_eTRaB[3]
WAE_eTRaB[4]
WAE_eTLaB[1]
WAE_eTLaB[2]
WAE_eTLaB[3]
WAE_eTLaB[4]
H166
INS007
Fig1-1-4-1-2_Write_Adress_Enable2
WAE_ea
J120e
J92e
J121e
J97
RBED_e
RBED_e
RBED_e
RBED_e
REN_eB
REN_eT
REN_eB
REN_eT
h93
h192
h157
h137
Fig1-1-4-1-4_Read_Bus_Equalize
h91
h156
INS002
Fig1-1-4-1-3_NAND_Circuit
h146
h143
h145
J86
H140
H159
H161
J74e
J83e
J125
INS003
Fig1-1-4-1-1_Control_Cirucuit1
H[55]
H[54]
h157
h137
H[52]
H[53]
H[155:152]
Fig1-1-4-1_Sense_Amp_Controll


H61
H158
H157
H131
H155
H153
H152
H154
j125
Fig1-1-4-1-1_Downtrol_Circuit1