Integrated Circuit Analysis Sample Report

Silicon on Insulator (SOI) Product

Manufacture : [redacted]
Package Marking : ----------[redacted]----------
Die Mark : [redacted]----------
Die size : 6.00mm x 6.15mm = 36.9mm^2

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Contents

1. Package image

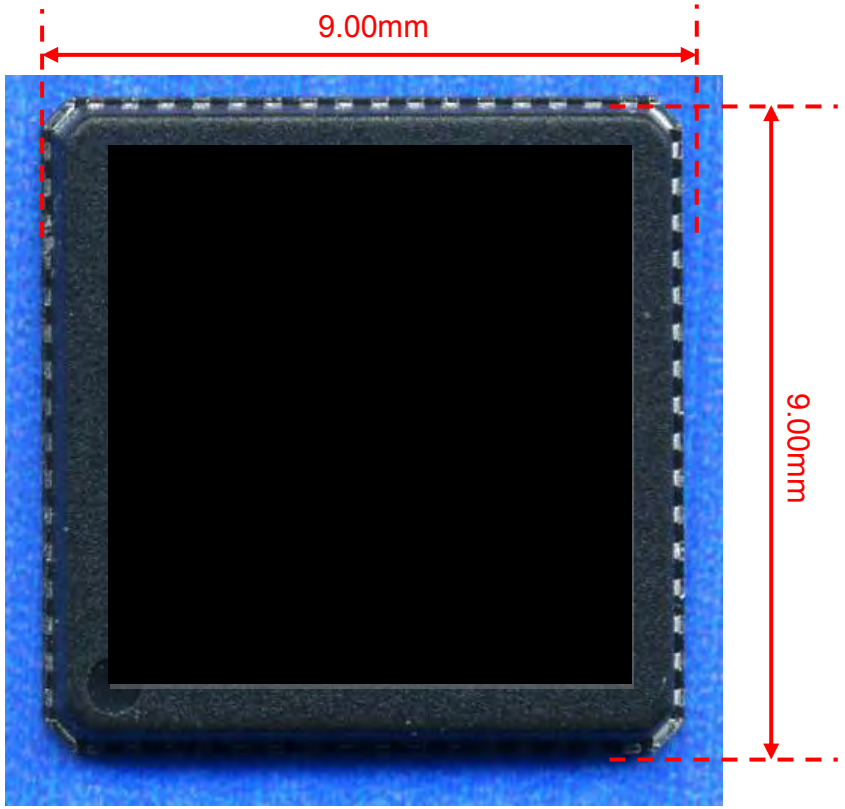


Fig.1-1 Package (Top View)

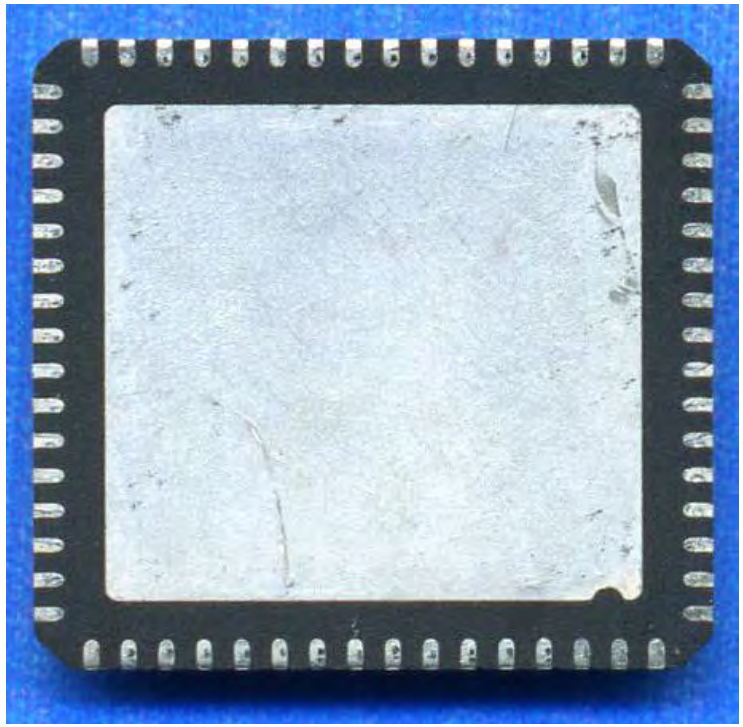


Fig.1-2 Package (Bottom View)

2. X-Ray image

Fig.2-1 Package (Top View)

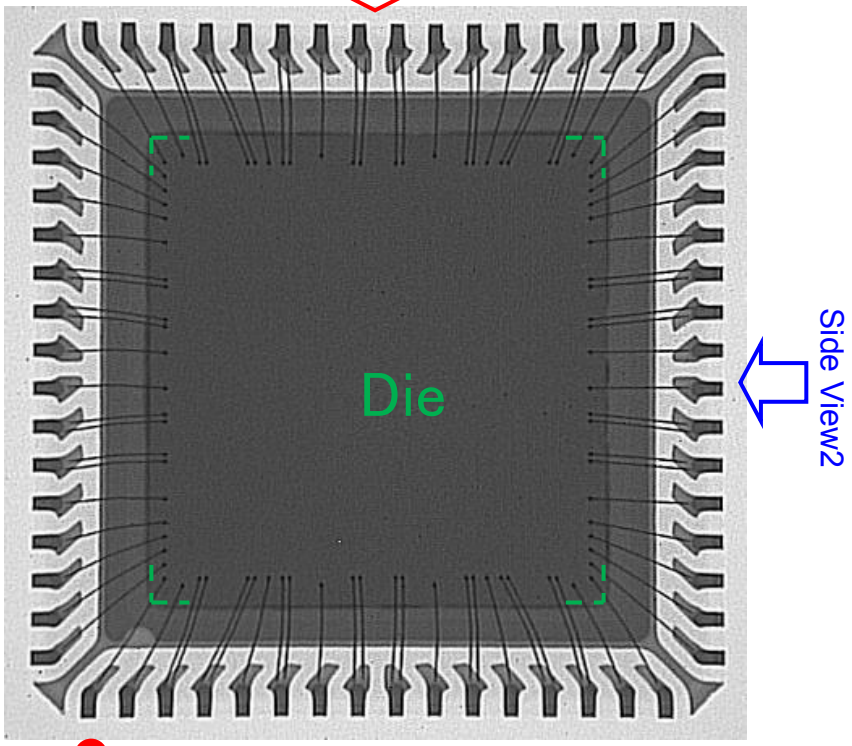


Fig.2-2 X-Ray image (Top View)

Fig.2-3 X-Ray image (Side View1)

Fig.2-4 X-Ray image (Side View2)

3. Die overview

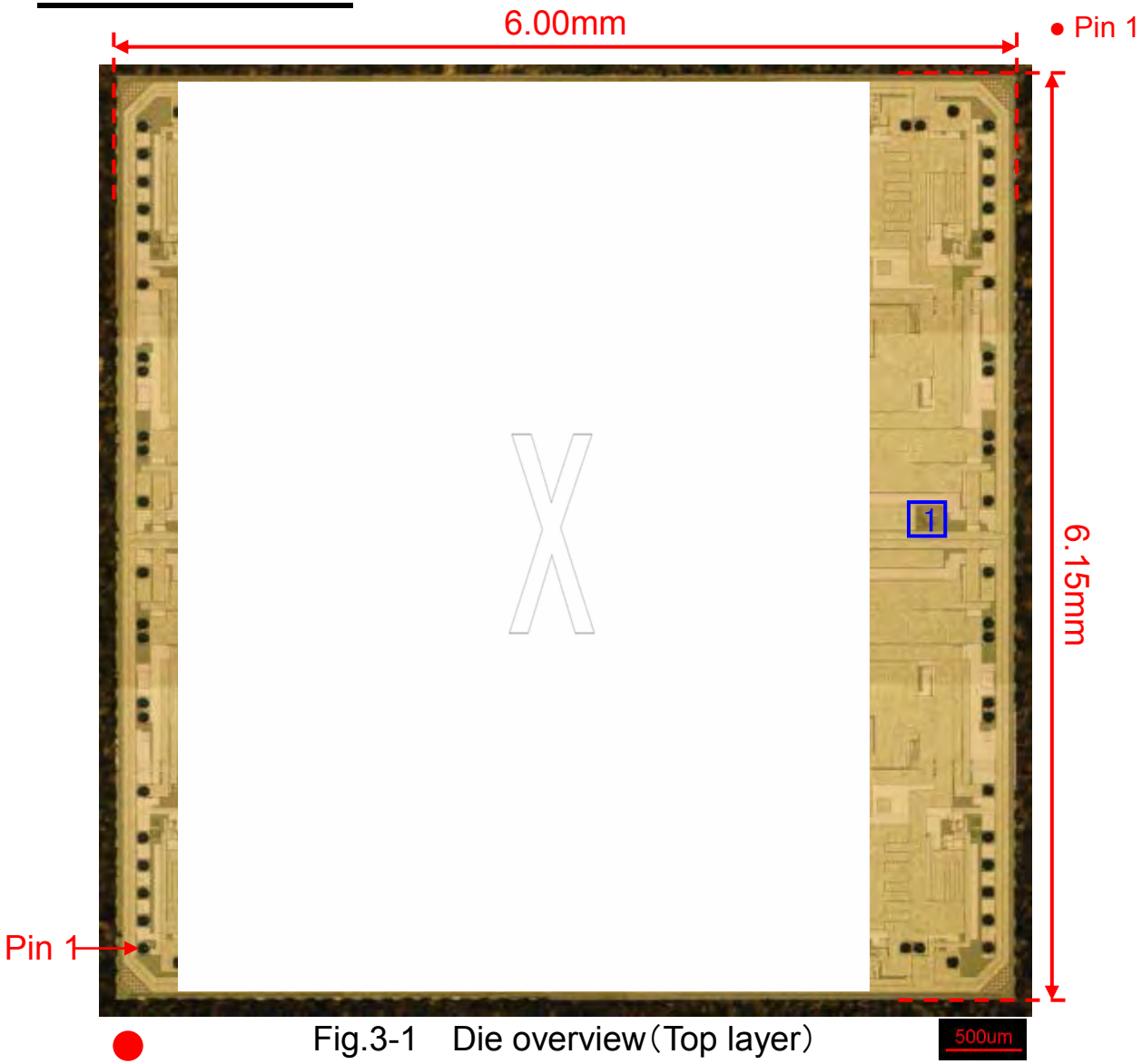


Fig.3-1 Die overview（Top layer）

※rotated 90°

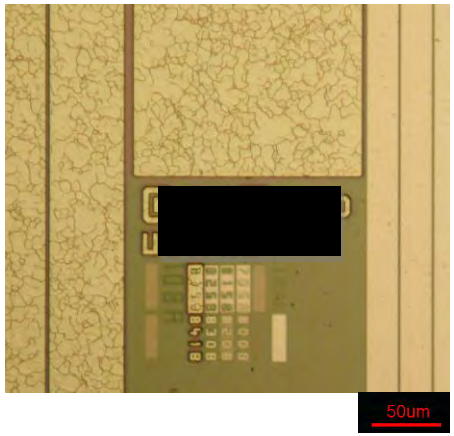


Fig.3-2 Die marking

- **Die size：**

  6.00mm×6.15mm = 36.9mm^2
- **Die mark：**

  XXX 2010 XXXX
- **Process：**

  0.35um CMOS, 4Metal 1Poly

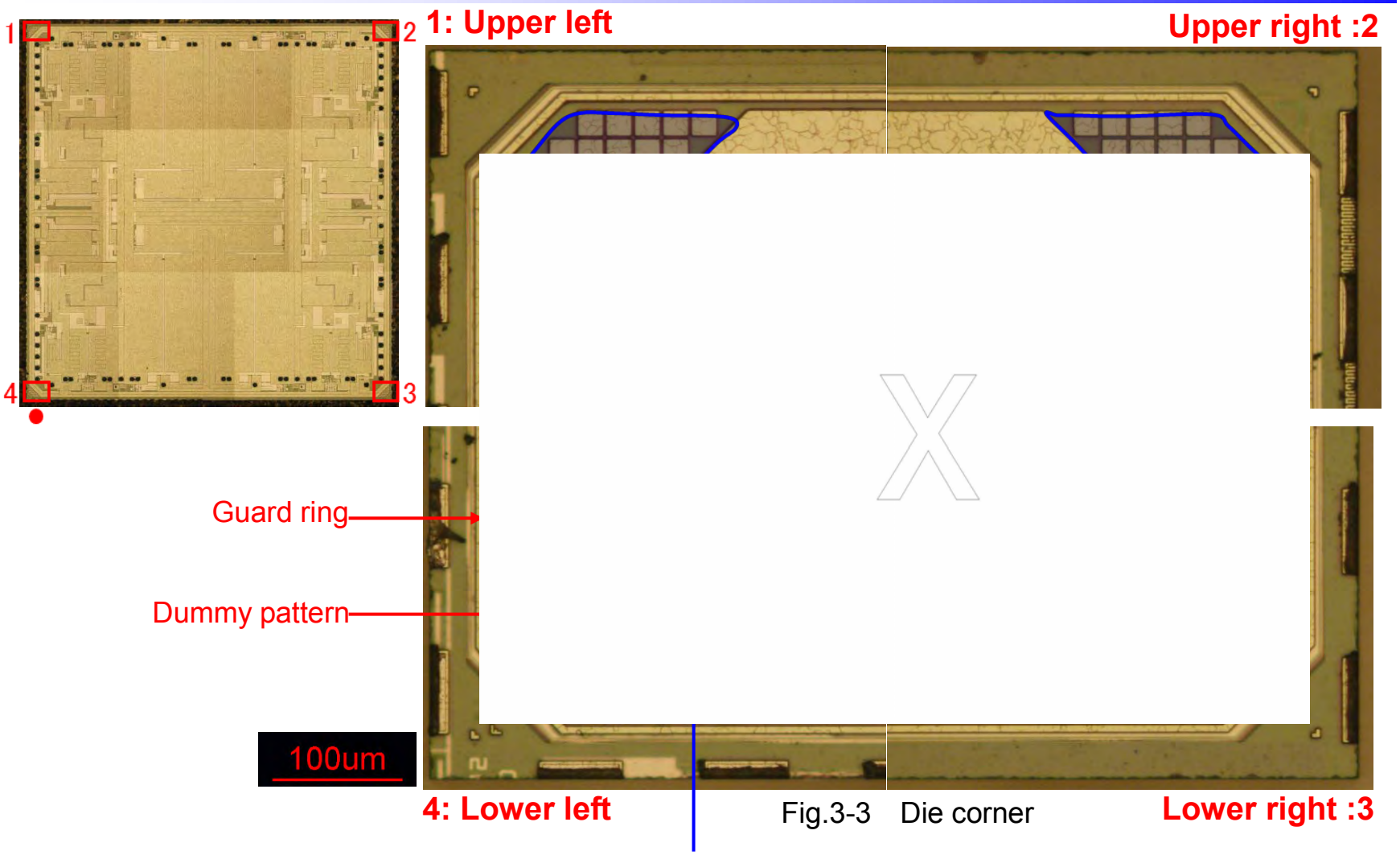


Fig.3-3 Die corner

Dummy patterns are placed at the die corners for stress relief.

4. Cross section analysis

4-0. Logic area and Pch/Nch power MOS locations

[redacted]

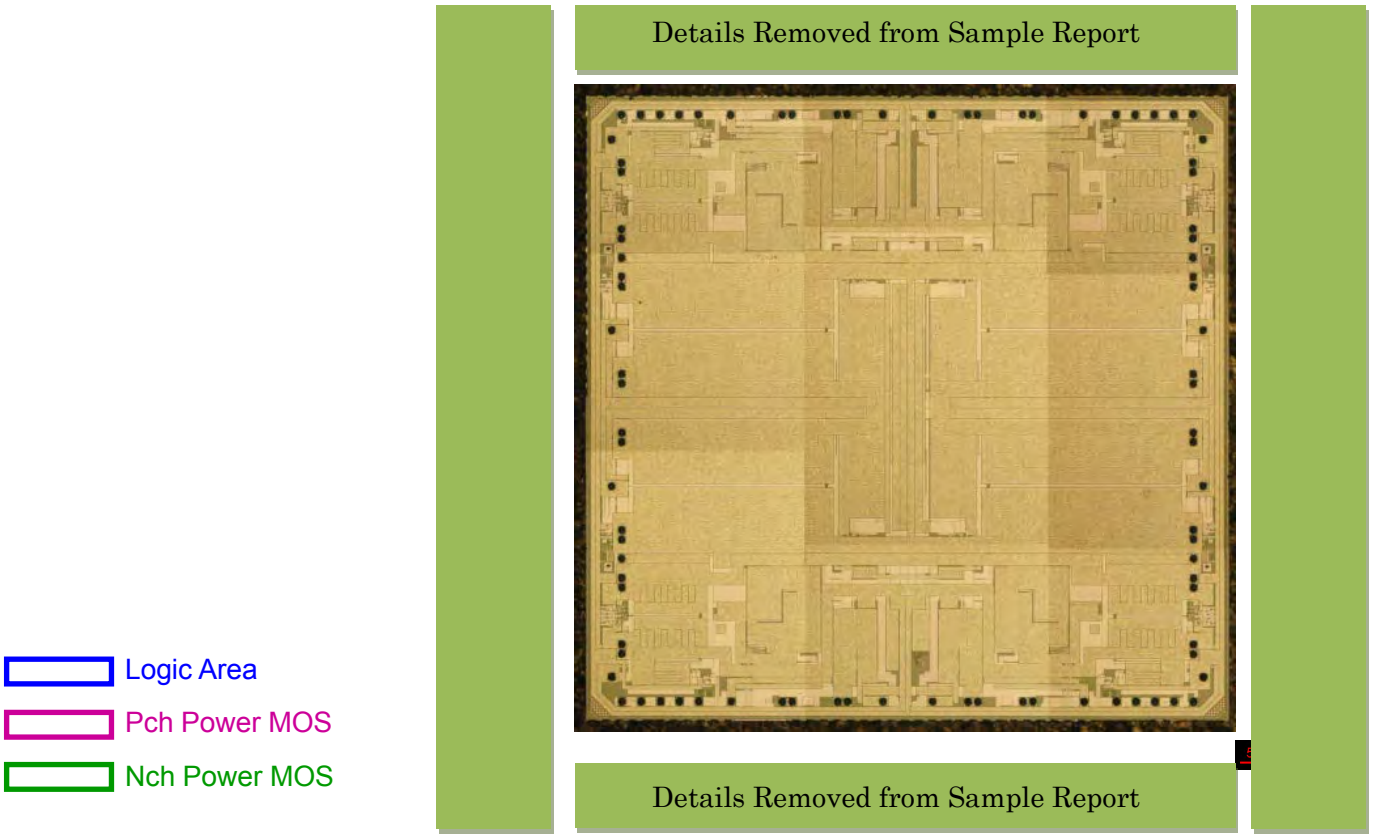
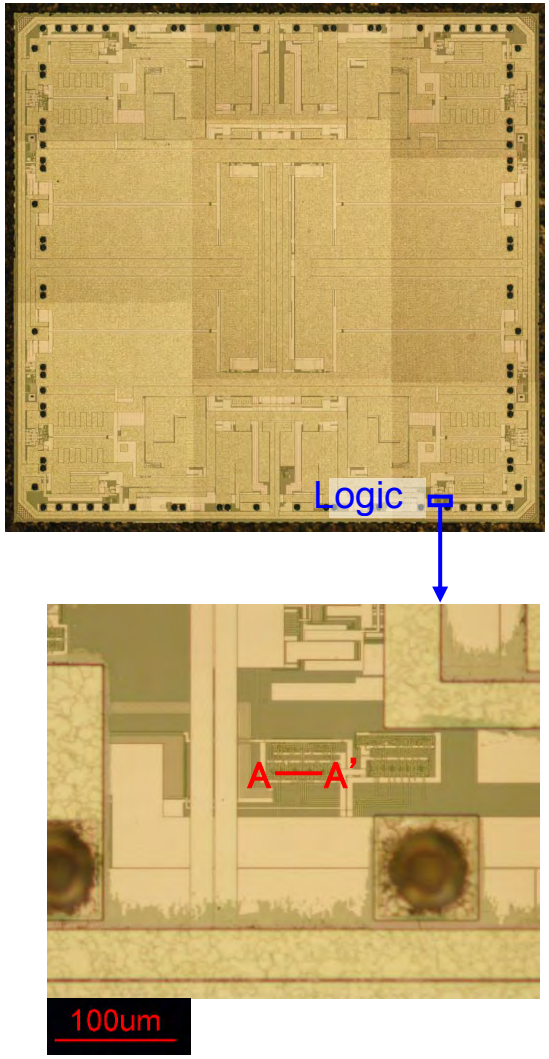


Fig.4-0-1 Locations of logic area and Pch/Nch power MOS

4-1. Logic area cross section

● Pin 1



※Tilt 30°

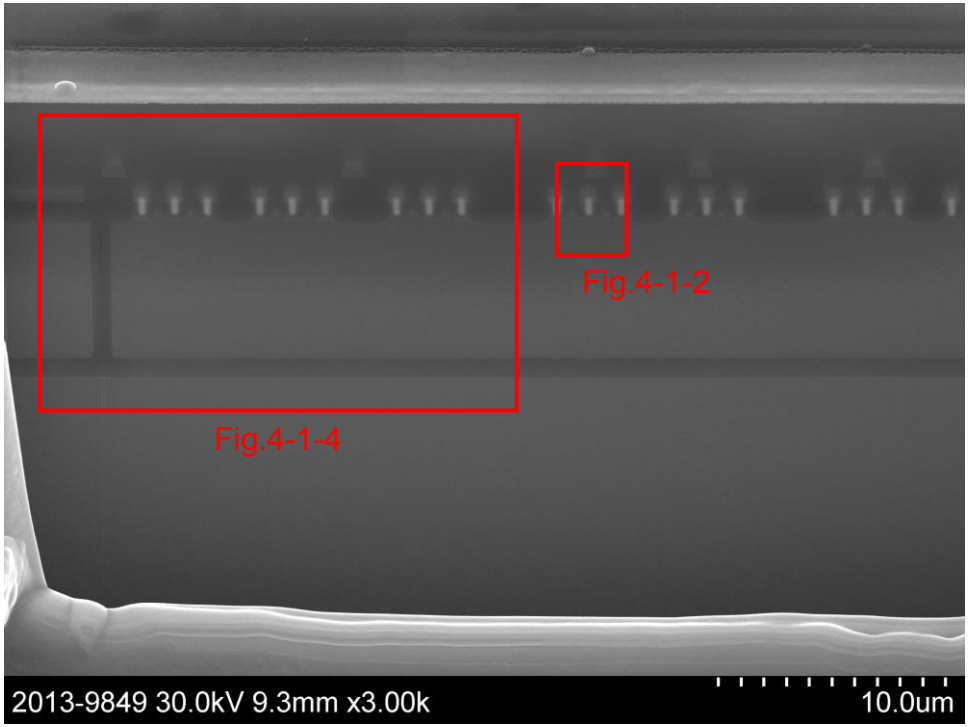


Fig.4-1-1 Logic cross section image (A-A')

※Tilt 10°

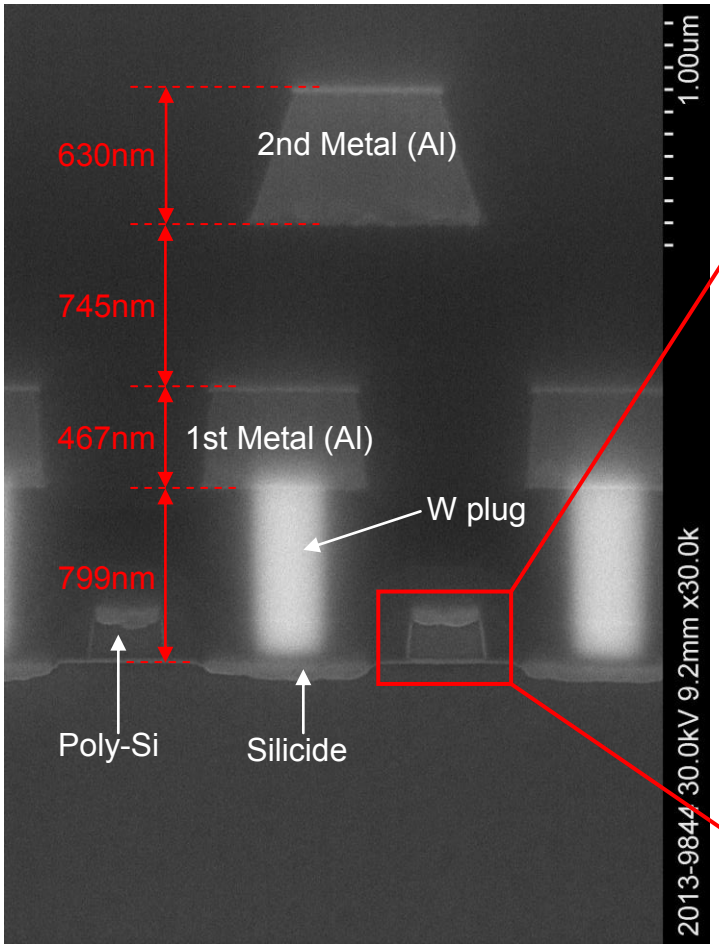


Fig.4-1-2 Logic cross section SEM image

※Tilt 10°

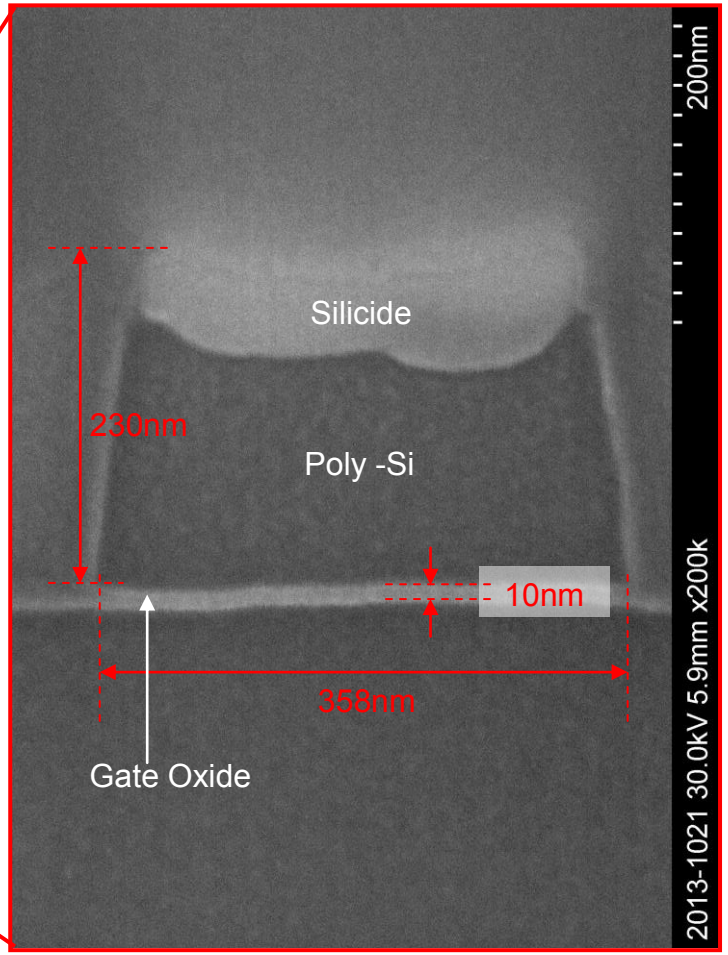


Fig.4-1-3 Poly-Si

・CMOS process rule of this die is estimated 0.35um process rule.

LTEC Applied chemical treatment to highlight the Epi layer (if any).

※Tilt 10°

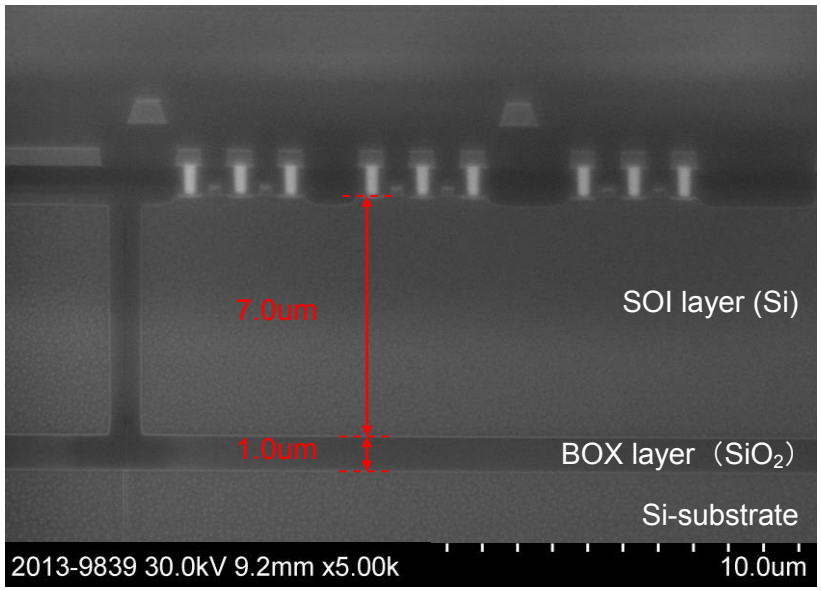


Fig.4-1-4　Before the chemical treatment

※Tilt 10°

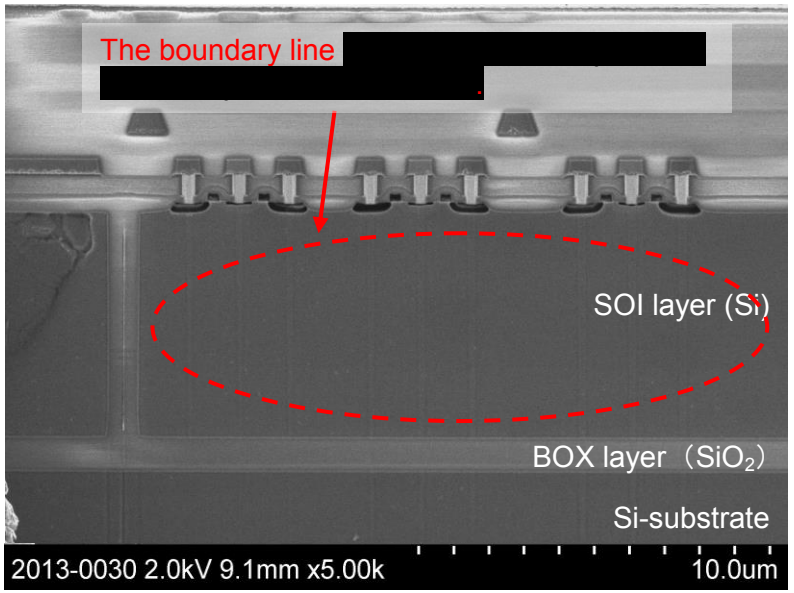


Fig.4-1-5　After the chemical treatment (Logic)

【Comments】

[redacted]

SOI layer and the Epi

- **The boundary line between the SOI layer and the Epi layer was not found.**

・Our opinion is that [redacted]**.**

There is [redacted]

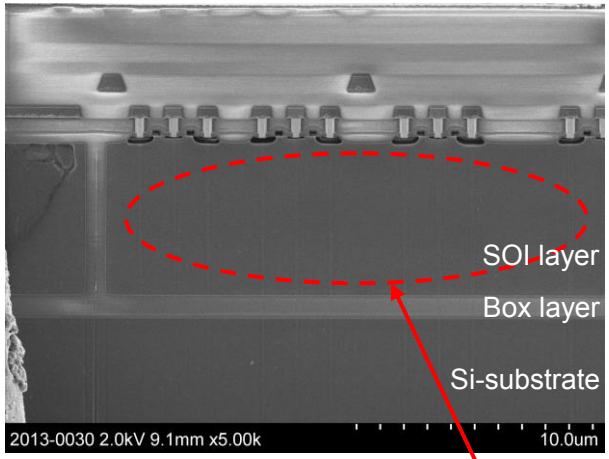


Fig.4-1-6
After the chemical treatment（Logic）

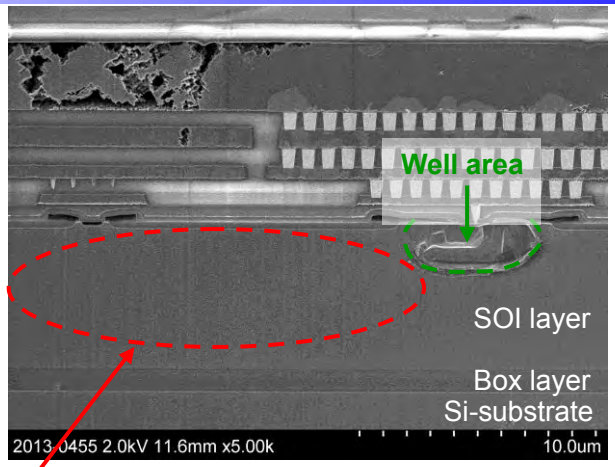


Fig.4-1-7
After the chemical treatment（Pch power MOS）

The [redacted]

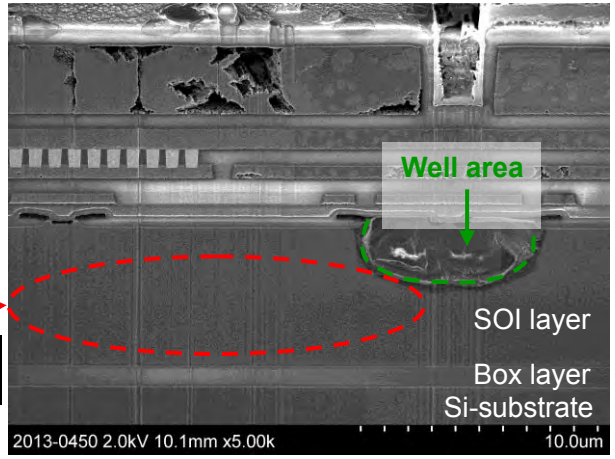


Fig.4-1-8
After the chemical treatment（Nch power MOS）

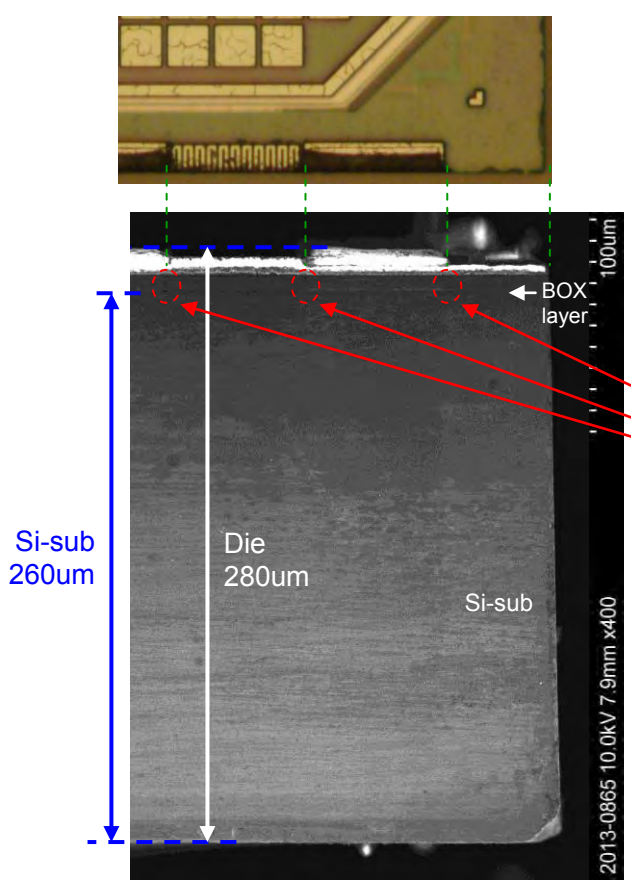


Fig.4-1-9 Die side SEM image

※Tilt 10˚

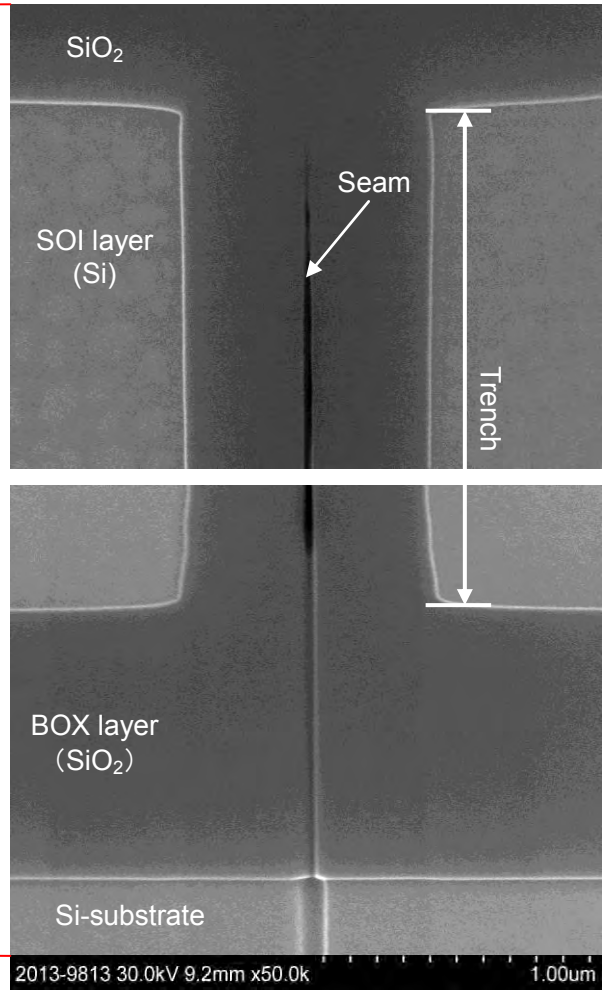
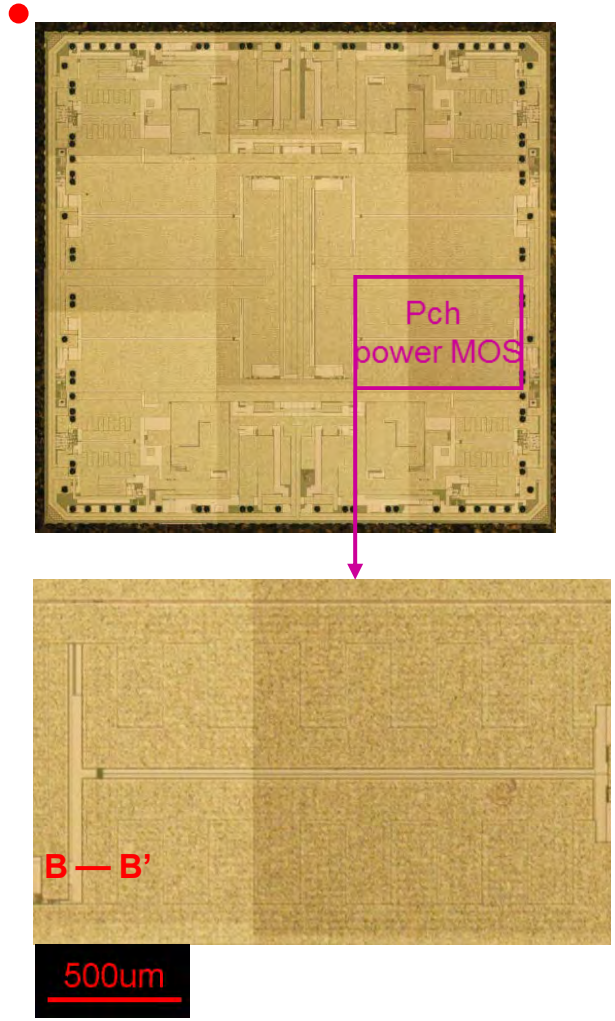


Fig.4-1-10 SOI cross section SEM image

Comments

4-2. Pch power MOS cross section



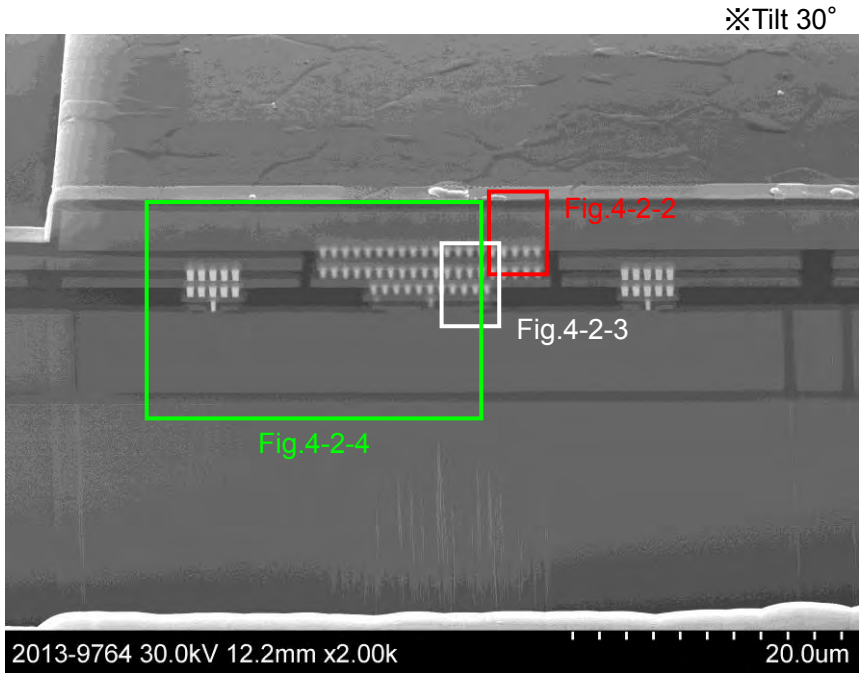


Fig.4-2-1 Pch power MOS cross section SEM image (B-B')

∗Tilt 10°

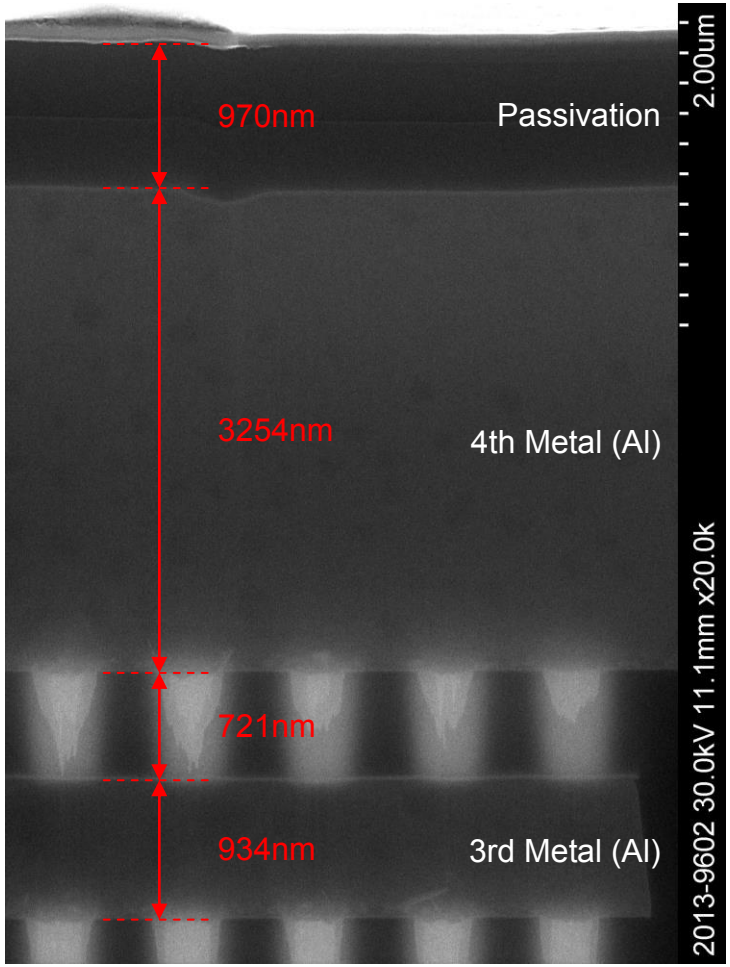


Fig.4-2-2 Pch power MOS cross section SEM image 1

∗Tilt 10°

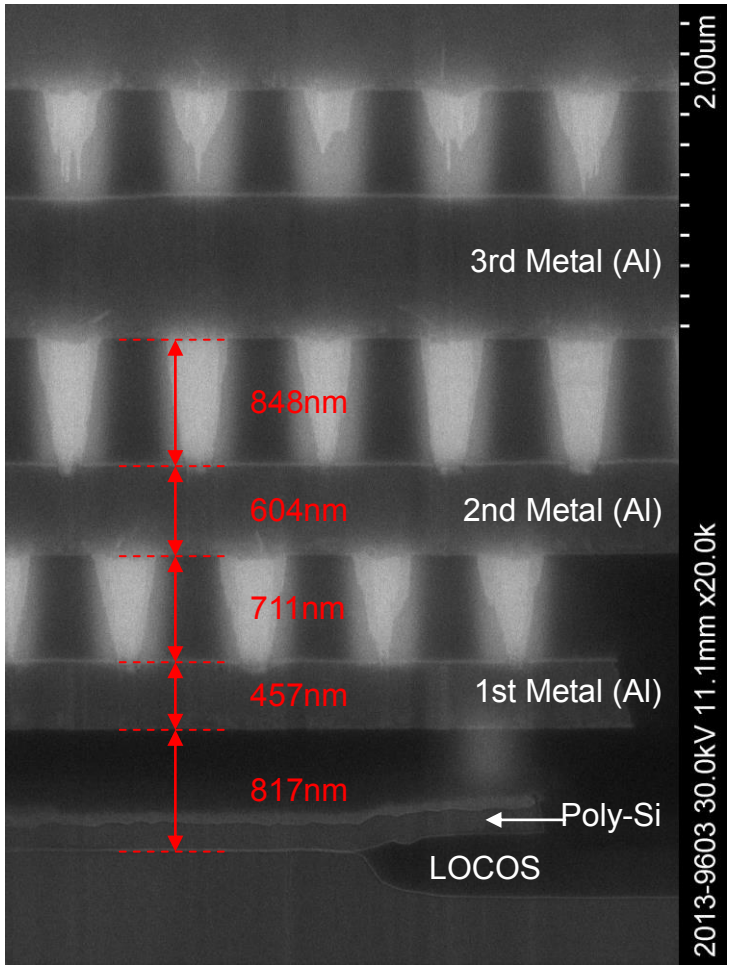


Fig.4-2-3 Pch power MOS cross section SEM image 2

※Tilt 10°

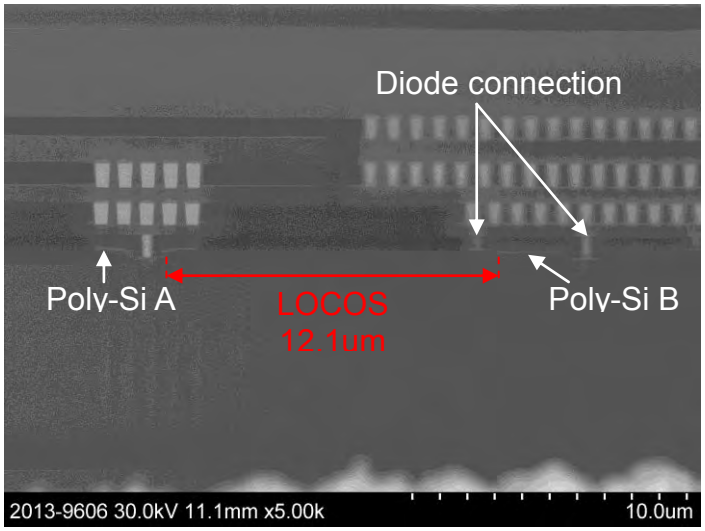


Fig.4-2-4　Pch power MOS cross section SEM image 3

Comments

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∗Tilt10°

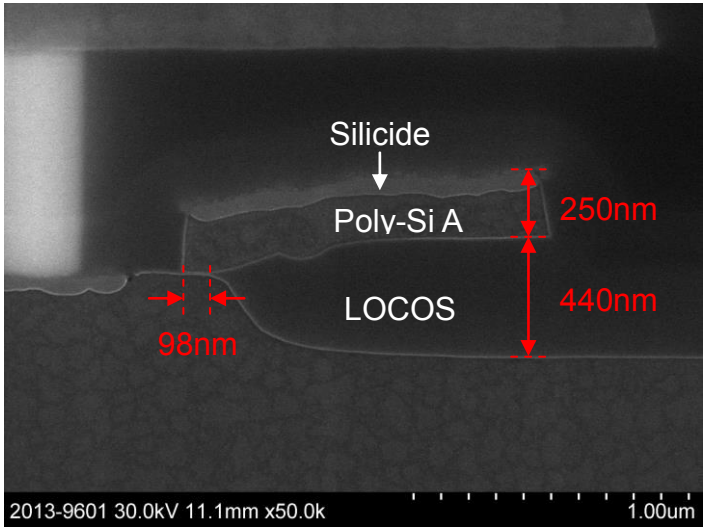


Fig.4-2-5　Poly-Si A

∗Tilt10°

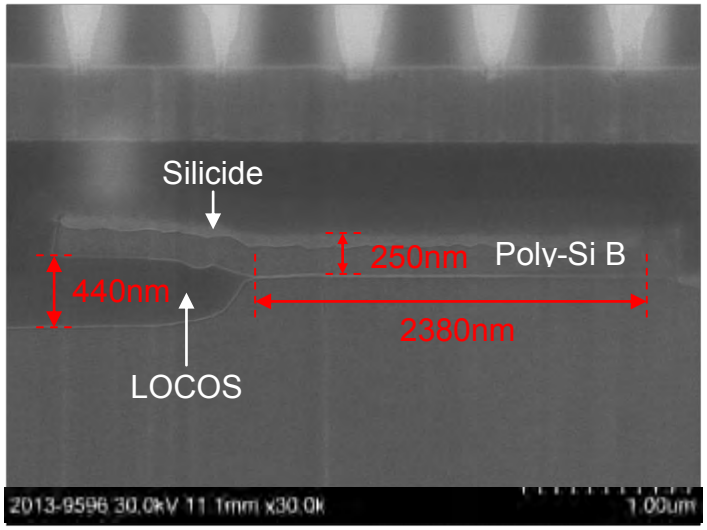
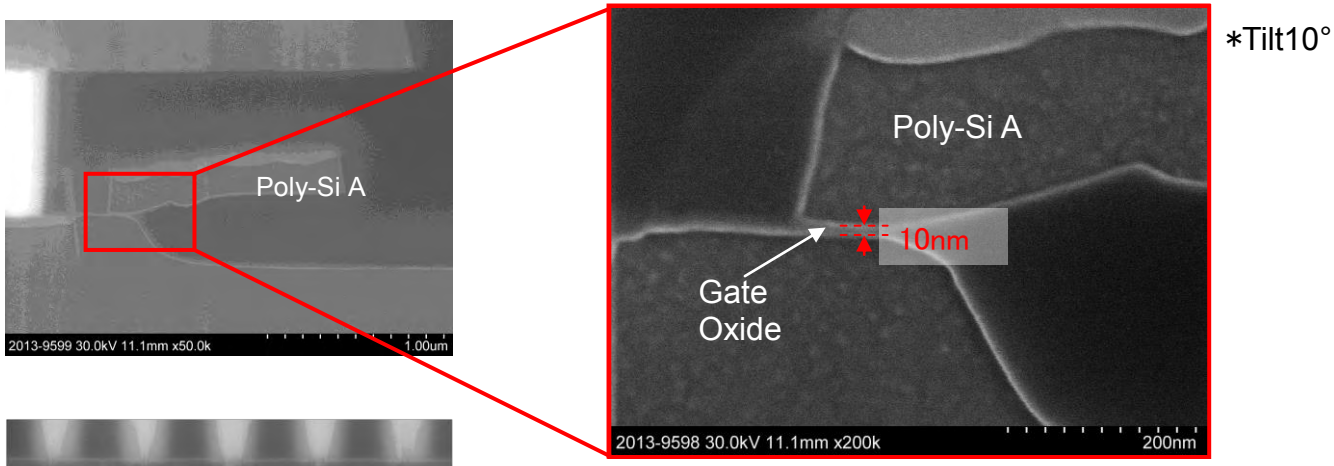
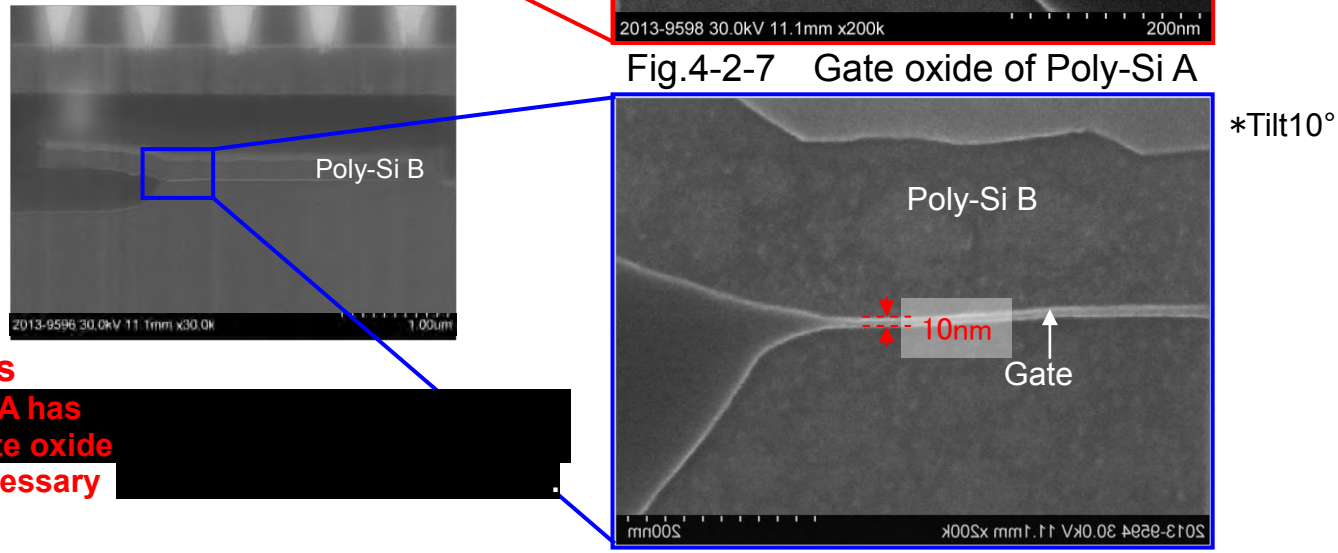


Fig.4-2-6　Poly-Si B



*Tilt10°

Fig.4-2-7 Gate oxide of Poly-Si A



*Tilt10°

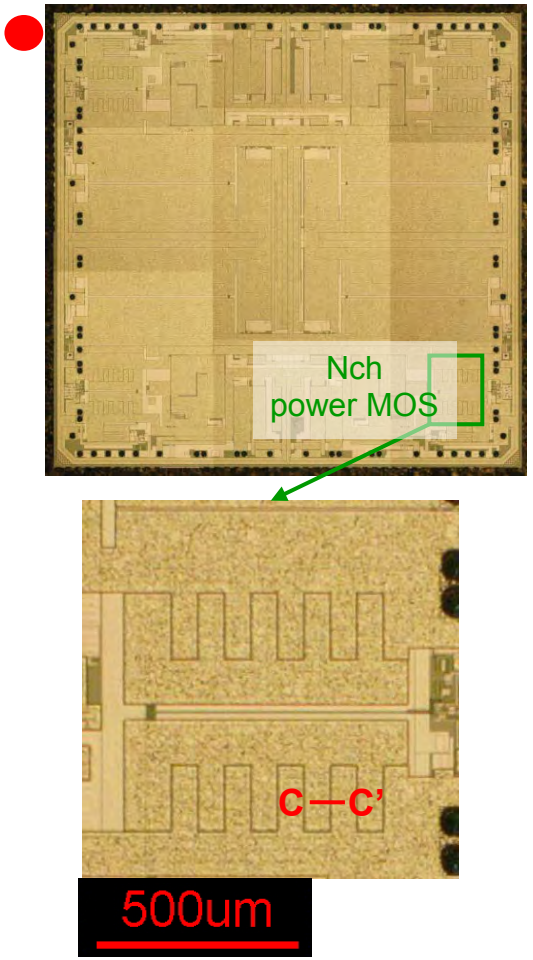
Fig.4-2-8 Gate oxide of Poly-Si B

Comments

- **Poly-Si A has**
- **This gate oxide**
- **It is necessary**

4-3. Nch power MOS cross section

- Pin 1



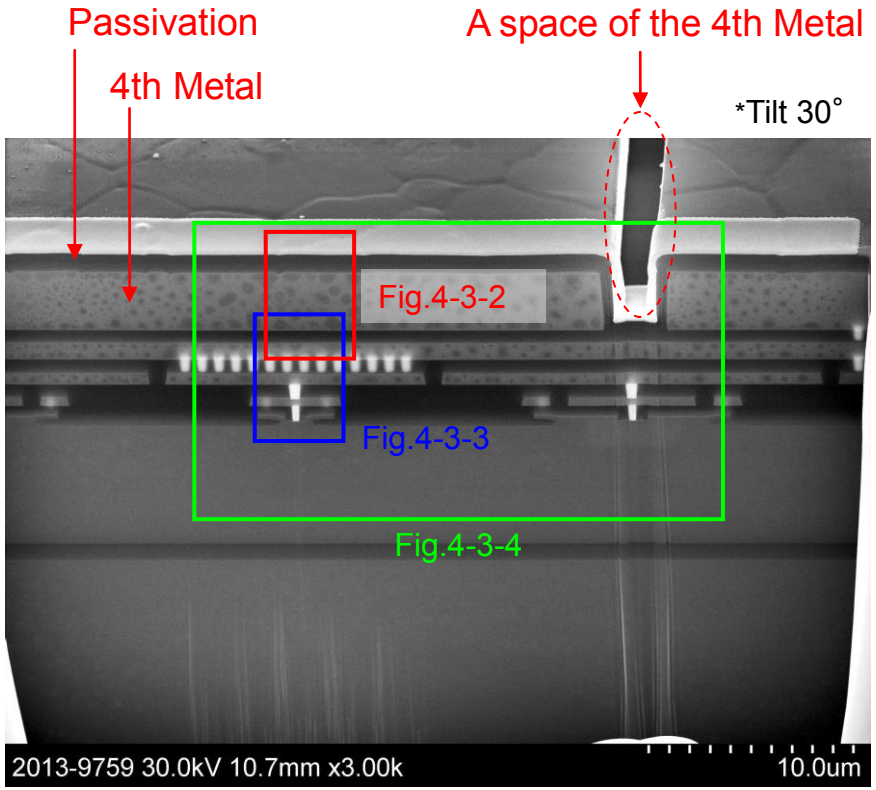


Fig.4-3-1 Nch power MOS cross section SEM image (C-C')

*Tilt 10°

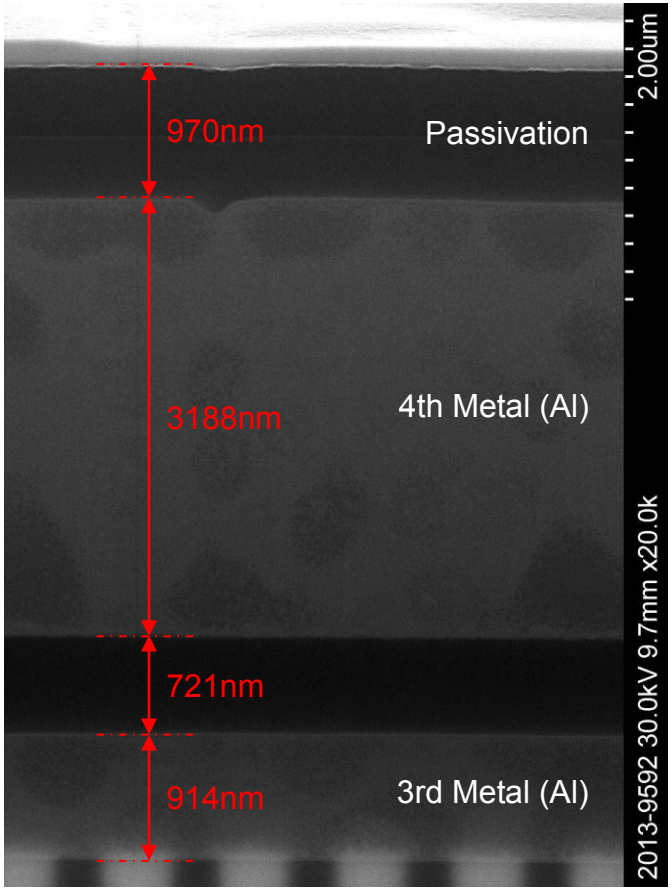


Fig.4-3-2 Nch power MOS cross section SEM image 1

*Tilt 10°

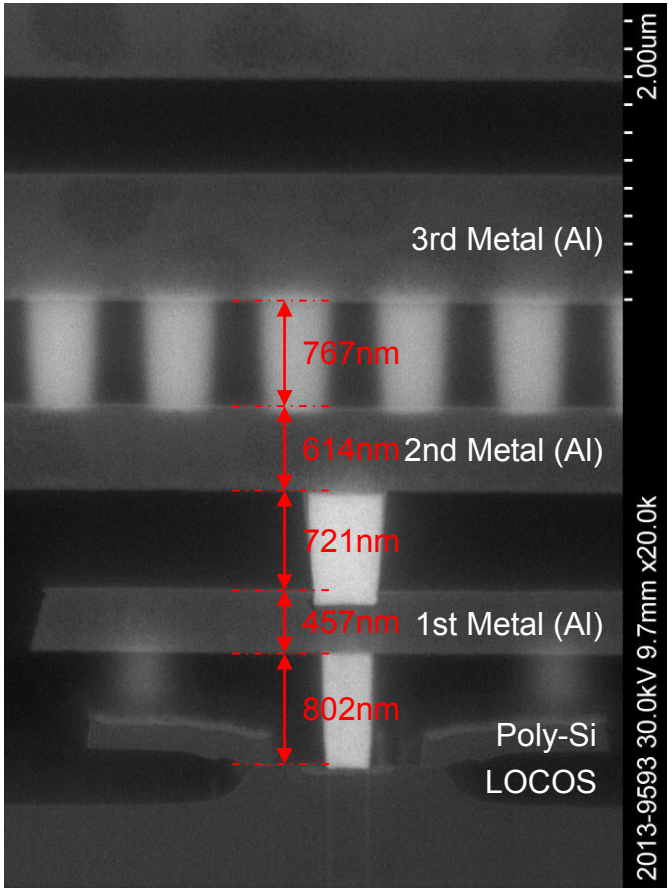


Fig.4-3-3 Nch power MOS cross section SEM image 2

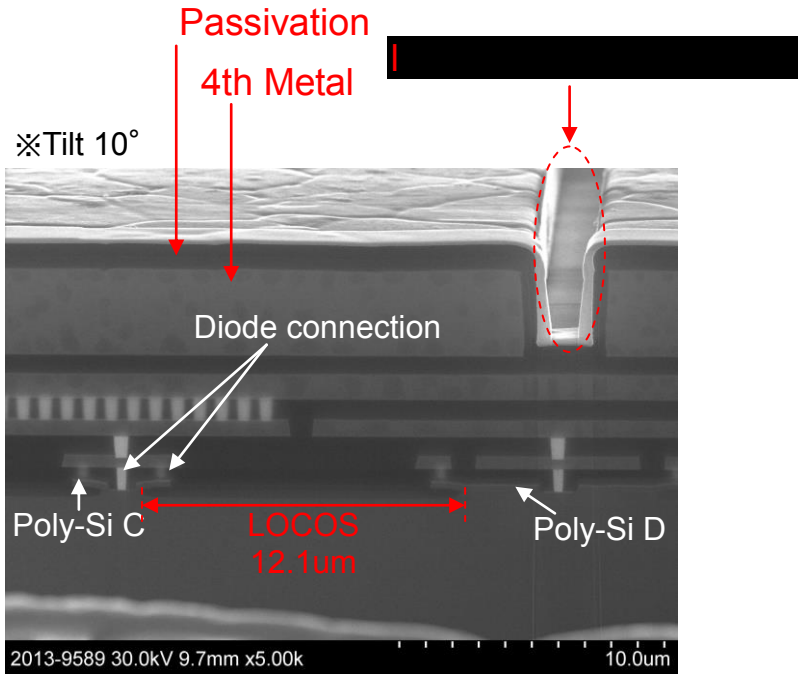


Fig.4-3-4 Nch power MOS cross section SEM image 3

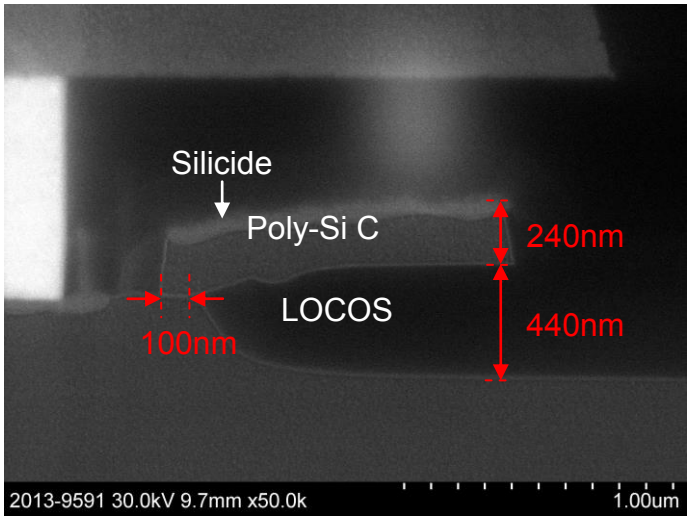


Fig.4-3-5 Poly-Si C

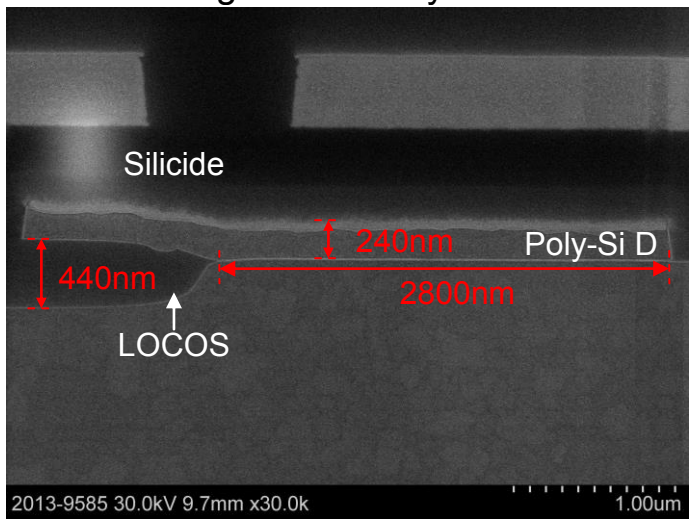
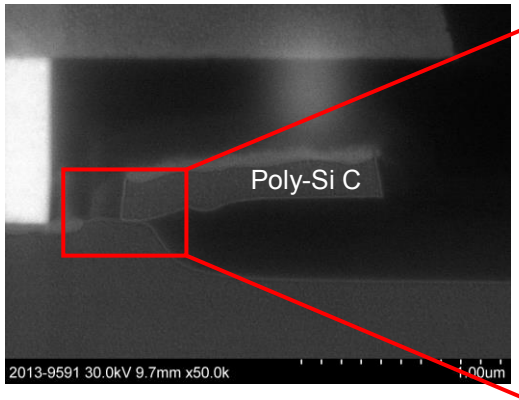
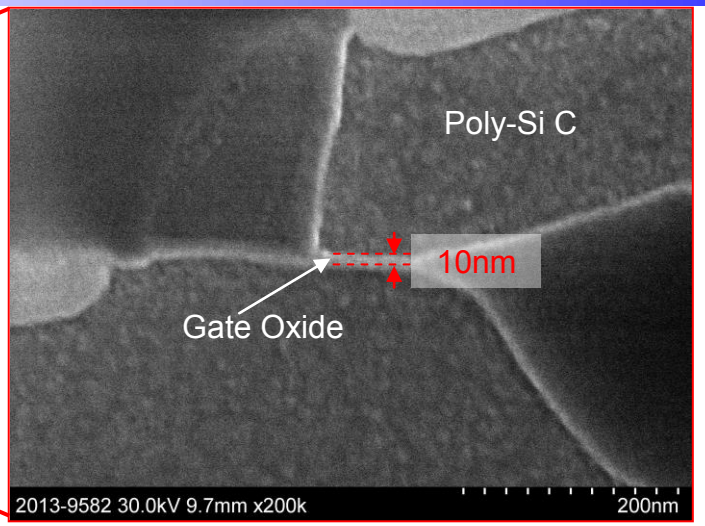


Fig.4-3-6 Poly-Si D

Comments

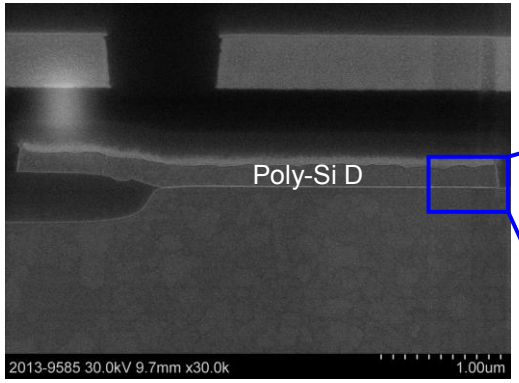
- **The LOCOS [redacted]**
- **Adjacent transistor has [redacted].**
- **Poly-Si D [redacted].**
- **We estimate that [redacted].**

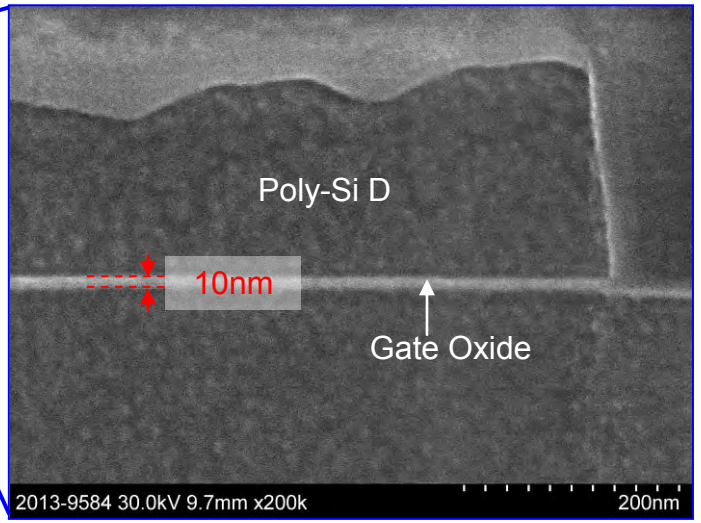




*Tilt10°

Fig.4-3-7 Gate oxide of Poly-Si C





*Tilt10°

Fig.4-3-8 Gate oxide of Poly-Si D

Comments

- **Poly-Si C** [redacted].
- **This gate** [redacted]
- **It is** [redacted]
- [redacted].

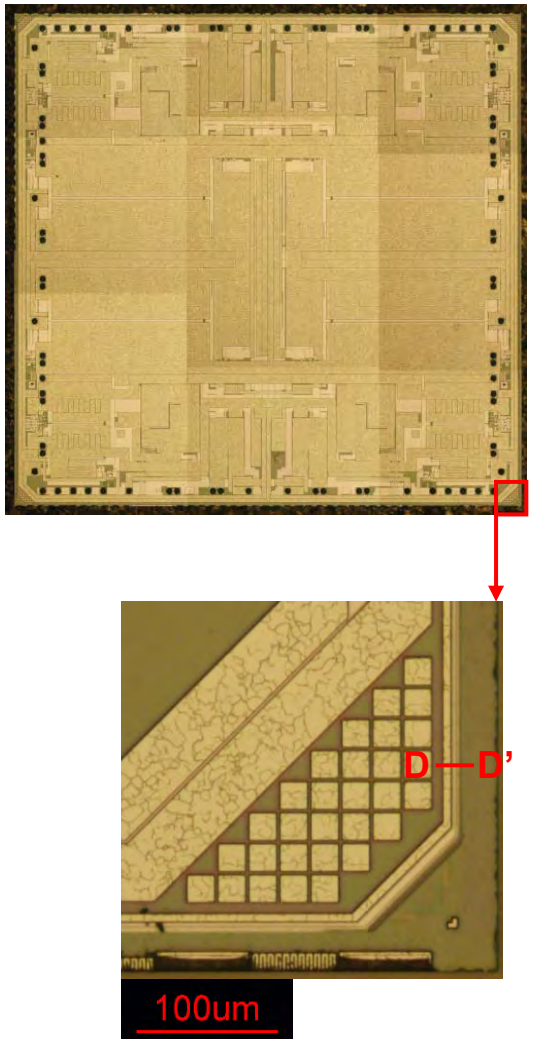
4-4. Layer thickness summary

Table.4-4-1 layer thickness

Measuring point	Thickness (nm)		
	Logic Area (※1)	Pch power MOS	Nch power MOS
Passivation	-	970	970
4th Metal	-	3254	3188
4th Metal - 3rd Metal ILD	-	721	721
3rd Metal	-	934	914
3rd Metal – 2nd Metal ILD	-	848	767
2nd Metal	630	604	614
2nd Metal – 1st Metal ILD	745	711	721
1st Metal	467	457	457
1st Metal – SOI ILD	799	817	802
Gate layer	230	250	240
LOCOS（*2）	-	440	440
Gate Oxide	20→10（*2）	10	10
SOI layer	7000	-	-
BOX layer	1000	-	-

*1 There are no 3rd and 4th Metal in the Logic Area.
*2 The writing in red identifies corrected or added items.

● Pin 1



- **In case [redacted].**
- **However [redacted].**
- **It contacts [redacted].**
- **It is estimated that [redacted].**

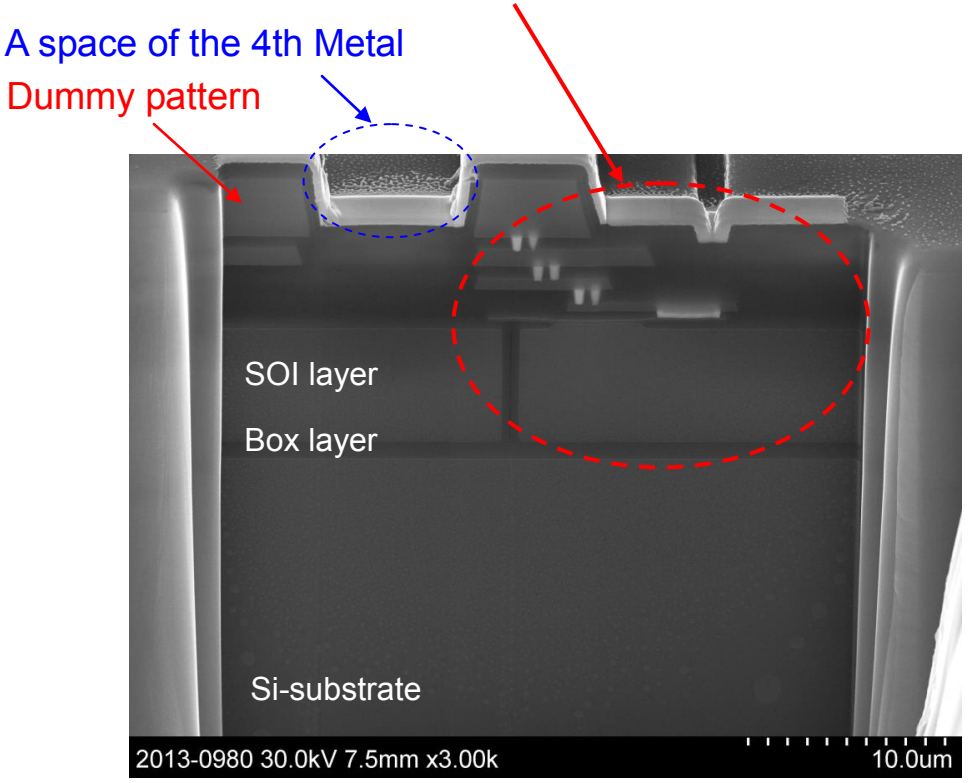


Fig.4-5-1 Shield area (seal ring) cross section SEM image (D-D')

- Pin 1

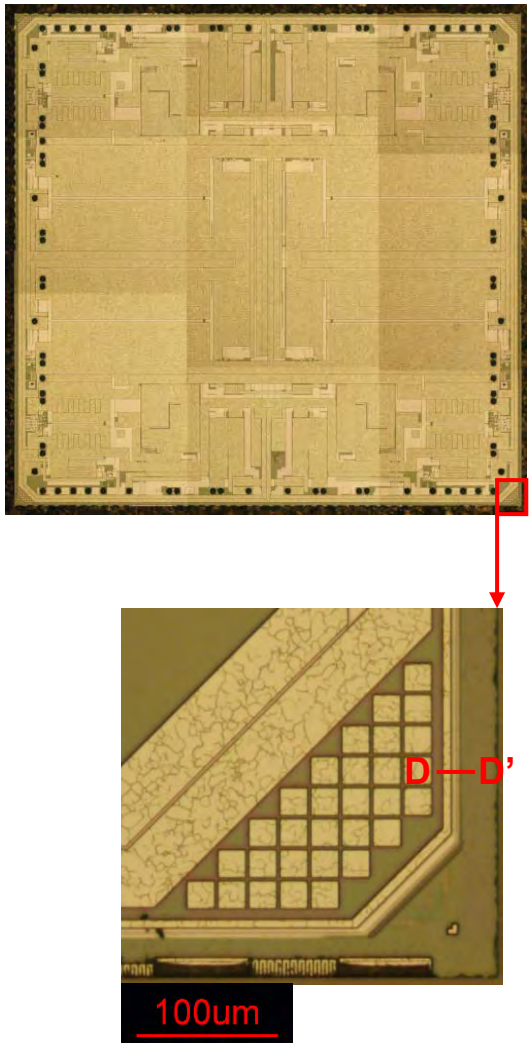


Fig.4-5-3

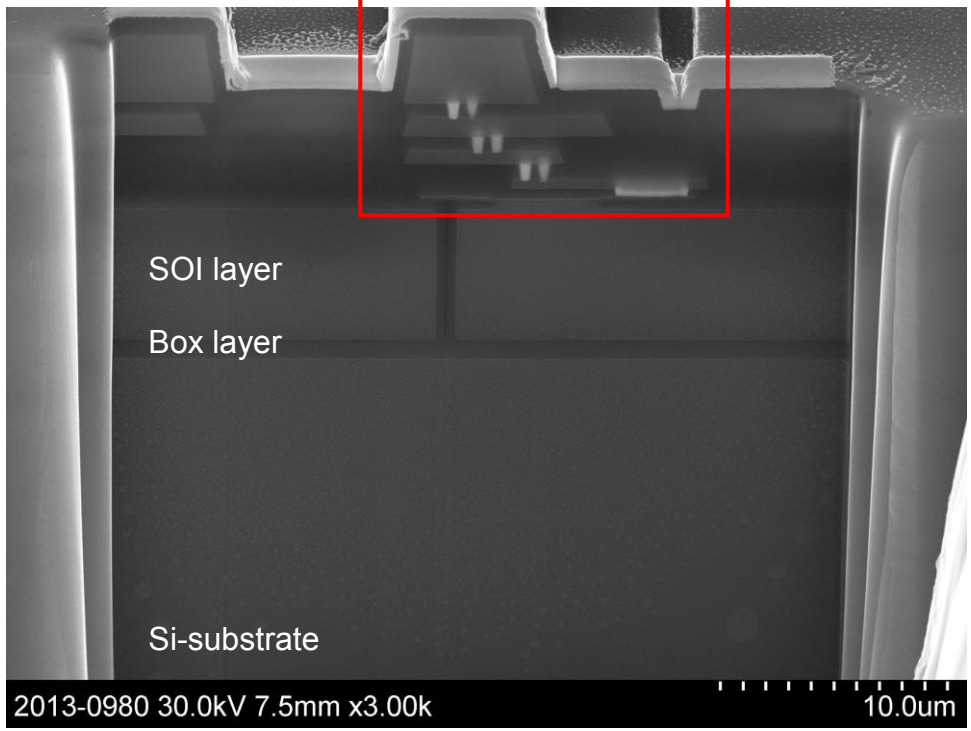


Fig.4-5-2 Shield area (seal ring) cross section SEM image (D-D')

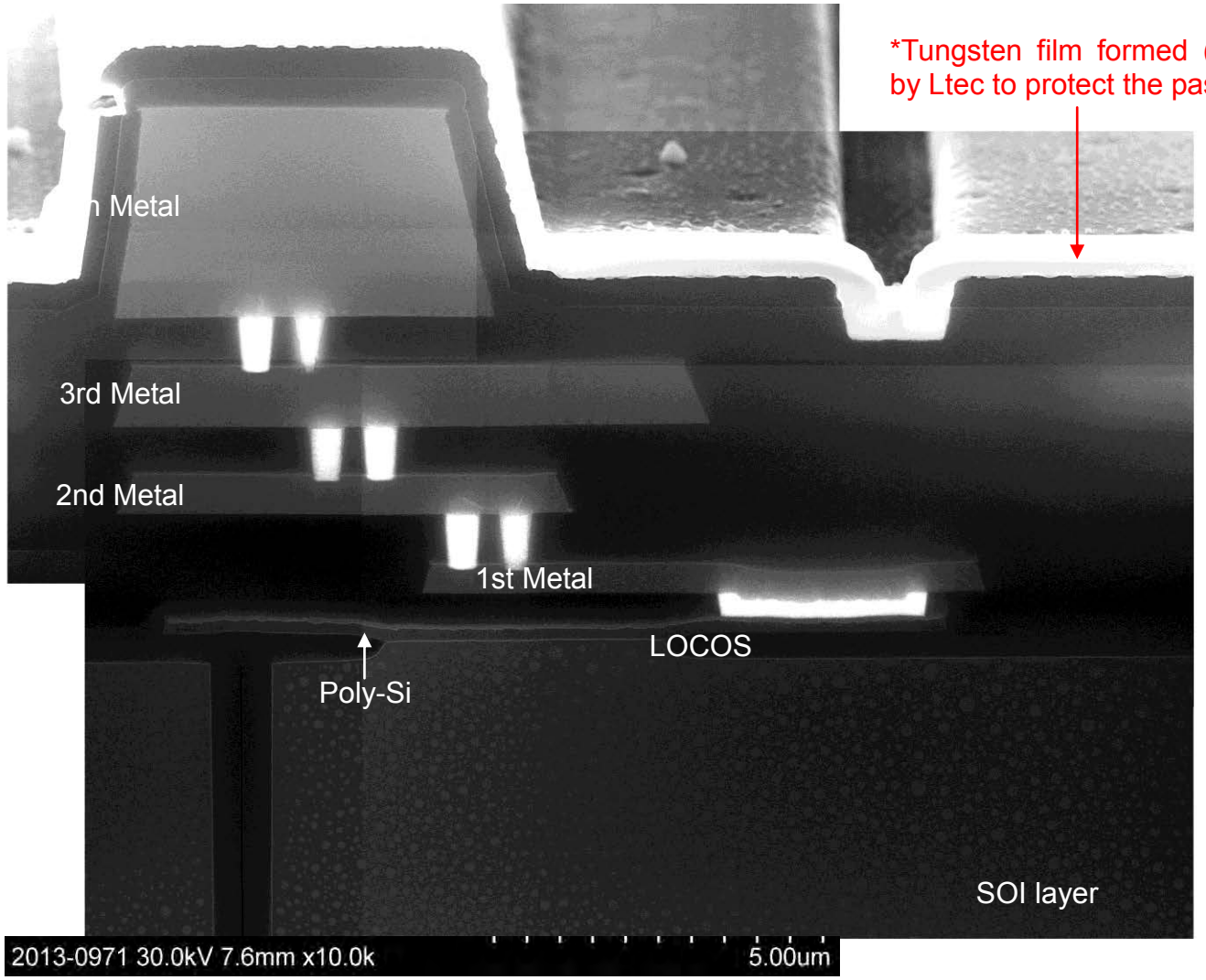


Fig.4-5-3 Shield area (seal ring)cross section SEM image

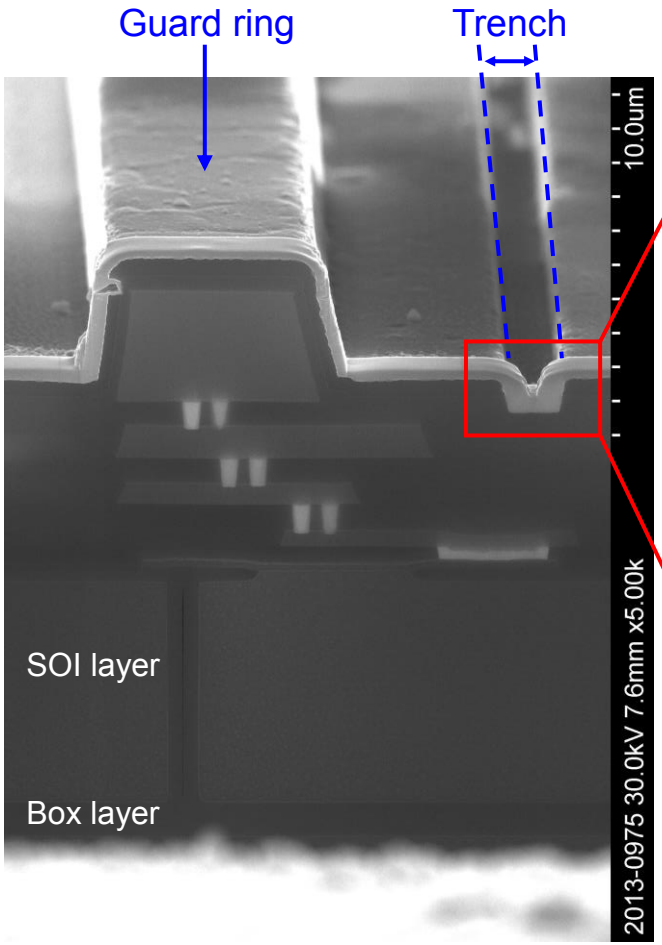


Fig.4-5-4　Shield area (seal ring) cross section SEM image

*Tungsten film formed (deposited) by Ltec to protect the passivation

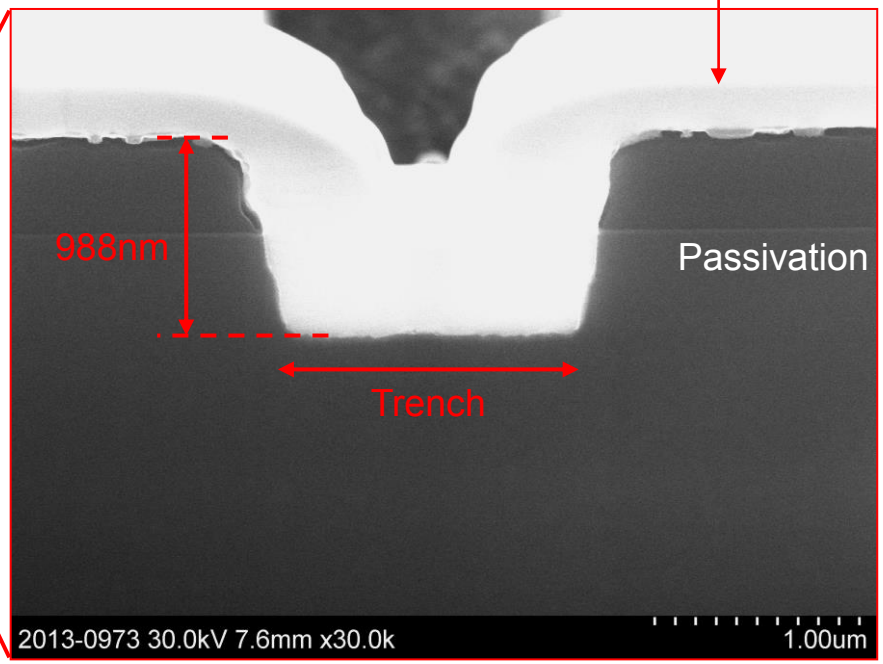


Fig.4-5-5　Shield area (seal ring) cross section SEM image (trench)

The trench is formed so as to surround the guard ring.

5. Ground contact

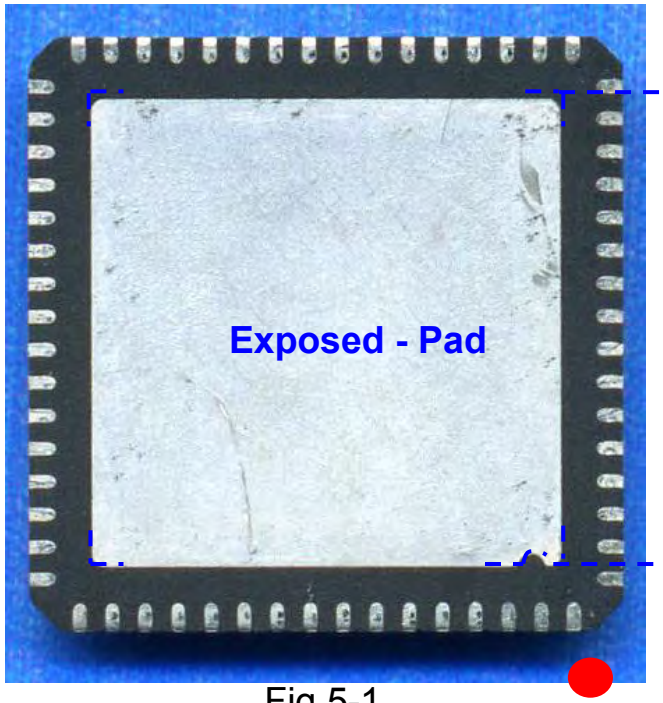


Fig.5-1
Pin numbers based on the datasheet pin configurations

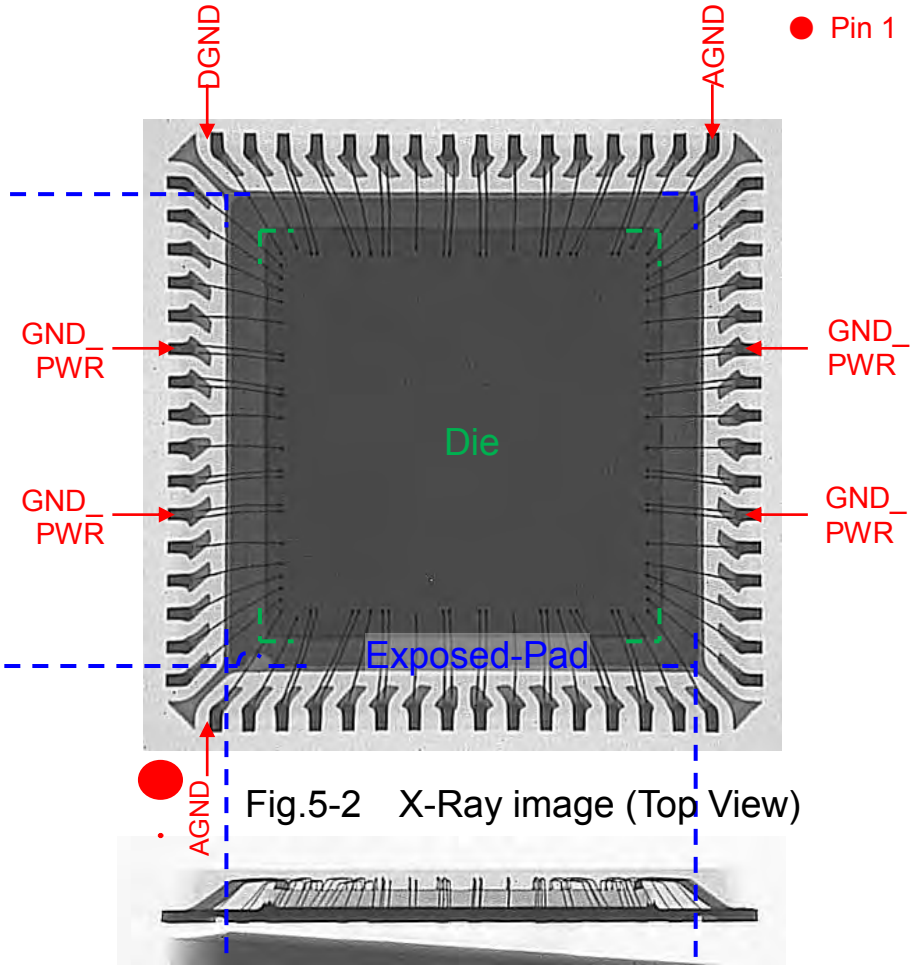
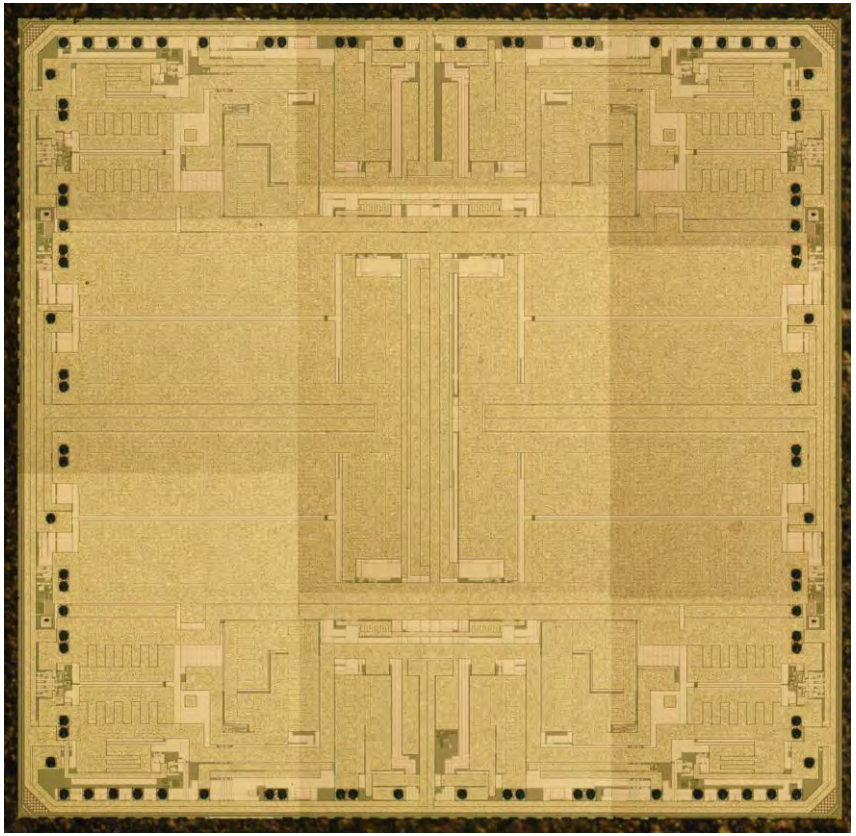


Fig.5-2 X-Ray image (Top View)

Fig.5-3 X-Ray image (Side View)

has 4 type ground pin.
AGND･･･Signal ground
DGND ･･･Logic ground
GND_PWR･･･Power ground
Exposed-Pad･･･Internally connected to the substrate
*The ground contact does not [redacted]

Details Removed from Sample Report

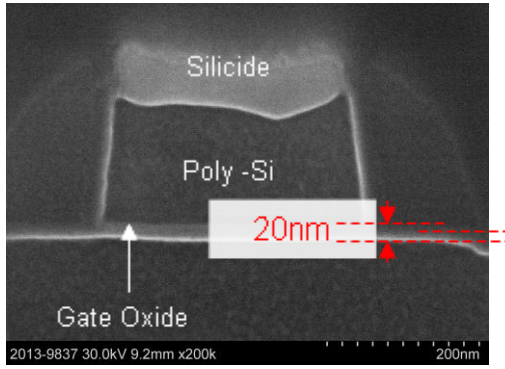


Details Removed from Sample Report

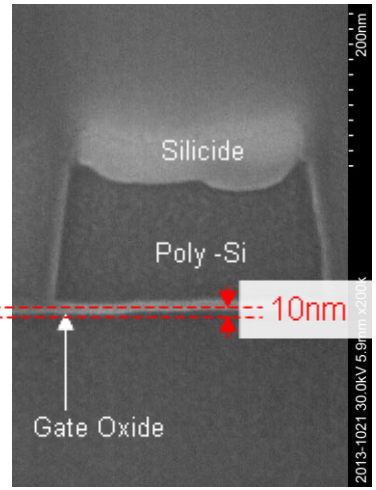
FiG.5-4 Pin configurations based on the datasheet

6. Gate oxide thickness in the logic area

Description about the gate oxide thickness in the logic area.



① 1st observation



② 2nd observation

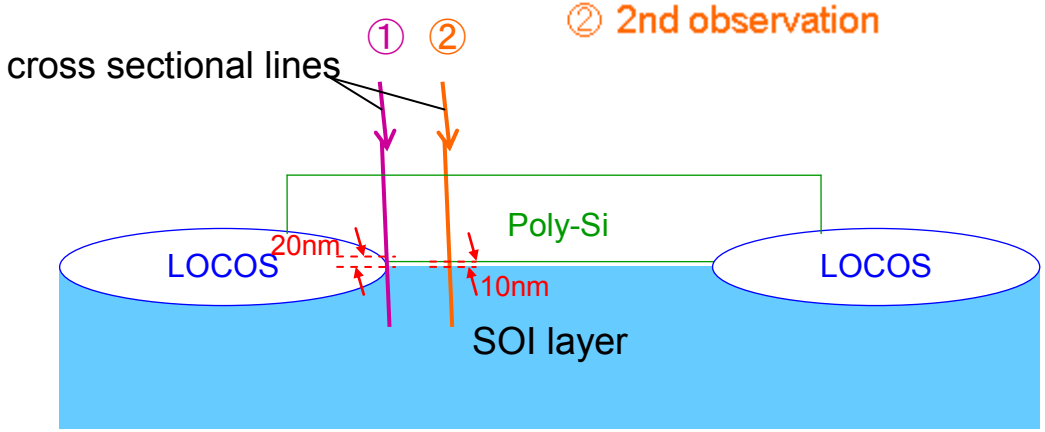
Problem

[redacted]

Reason

[redacted]

.



Solution

[redacted]

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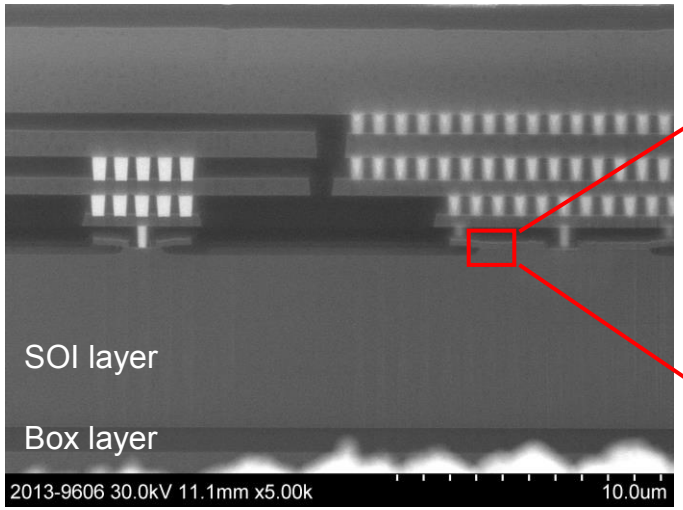
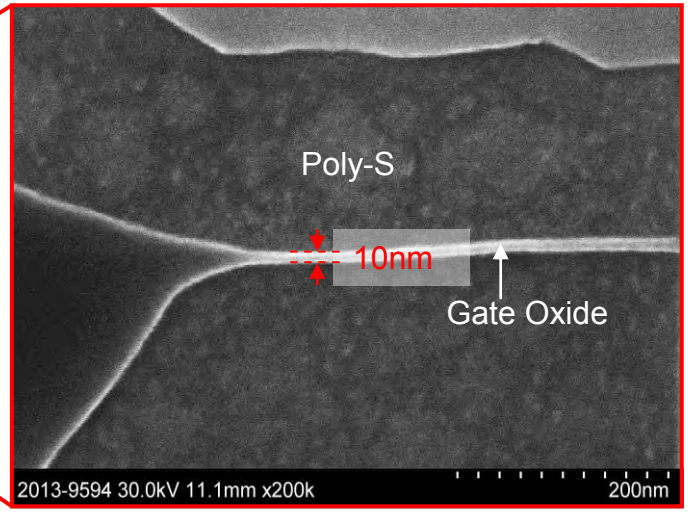
7. Gate oxide thickness in the power device Recommendation for further analysis

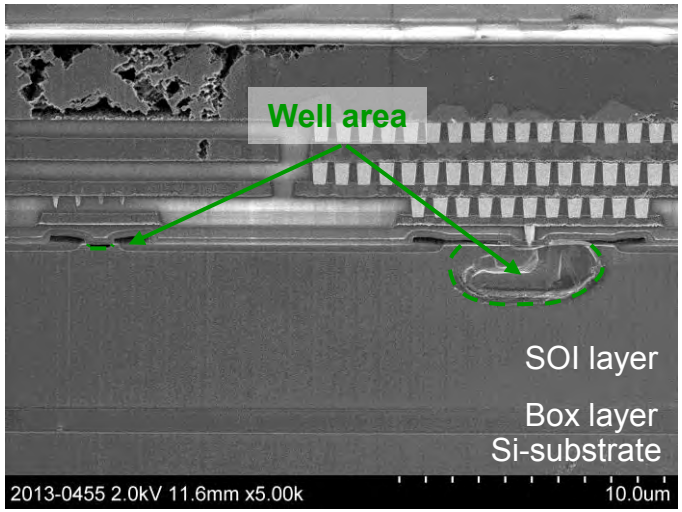
Power device



Before the chemical treatment（Pch power MOS）



Gate oxide thickness



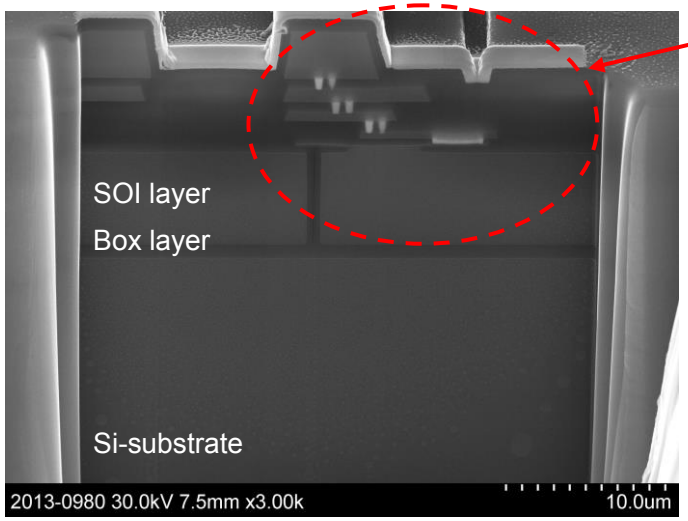
After the chemical treatment（Pch power MOS）

LTEC has confirmed that

LTEC recommends
1)
→
2)
→

8. GND (substrate) contact Recommendation for further analysis

Ground contact



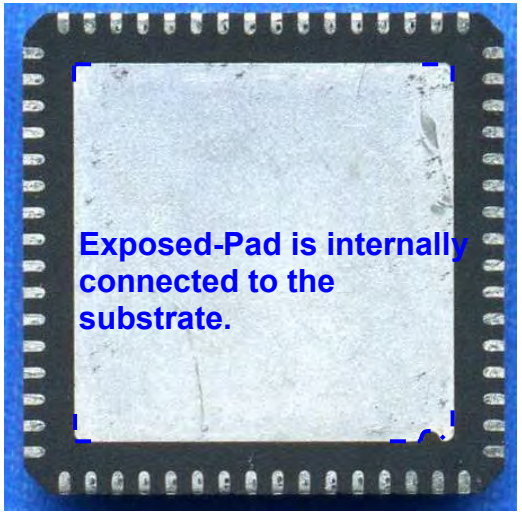
Shield area cross section SEM

[redacted]

Confirm [redacted]

Analysis:

- [redacted] → [redacted] →



9. Patent and literature search

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Content has been removed from Sample Report

LTEC has identified 497 Japanese patents, 433 has English language version, 64 patents are available in Japanese. All related to high-voltage SOI technology.

Ltec has identified and 82 Japanese publications that relate to high-voltage SOI technology.

In this Excel document we show examples of what was found, identify some key inventor companies and individuals, and make recommendations as to what types of further research could be done.

Pricing associated with individual tasks, has been provided.

10. High-voltage SOI products landscape in Japan

Report on competitive products in JAPAN (To xxxxxxxxxx-)

Content has been removed from Sample Report