

Buck Converter IC Circuit Analysis Sample Report

(Only selected portions are shown)

DEVICE	1000-mA, X-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER
Model Number	XXXXX
Maker	XXXXX
Package Marking	XXXXX
Chip Marking	1.29mm × 0.93mm = 1.20mm ²
Chip Size	3Metal-2Poly
Process	

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Contact in the USA:

LTEC Corporation US Representative Office
2280 Zanker Road No: 203
San Jose CA 95134

Phone: (408) 432-7247
Website: www.ltecusa.com
Contact: info@ltecusa.com

Headquarters:

LTEC Corporation
42-8, 4-chome, Higashiaroika, Itami-city, Hyogo, Japan

Table of Contents

Table1	Chip Information	10
<u>Introduction</u>		
Photo.1-1	Package (Top View)	11
Photo.1-2	Package (Bottom View)	11
Photo.2	X-Ray	12
Photo.3-1	Chip Overview	13
Photo.3-2	Chip Marking1	13
Photo.3-3	Chip Marking2	13
Photo.4-1	Pin Assignment (Bottom View)	14
Photo.4-2	Pin Assignment (X-Ray)	14
Photo.4-3	Pin Assignment (Chip Overview)	14
<u>Elements</u>		
Photo.5-1	MOS Transistor1	15
Photo.5-2	MOS Transistor2	16
Photo.5-3	HV-MOS Transistor1	17
Photo.5-4	HV-MOS Transistor2	18
Photo.5-5	Bipolar Transistor	19
Photo.5-6	Resistor1	19
Photo.5-7	Resistor2	20
Photo.5-8	Resistor3	20
Photo.5-9	Diode	21
Photo.5-10	Capacitor1	21
Photo.5-11	Capacitor2	22
Photo.5-12	EEPROM	23
<u>Analysis Area</u>		
Photo.6	Analysis Area	24
Table2	Function	24
Fig.0	Functional Block Diagram (from datasheet)	25
<u>Circuit</u>		
Fig.1	Top Block Diagram	26
Fig.2	Band-Gap Reference and Bias Supply	27
Fig.2-1	Band-Gap Reference	28
Fig.2-1-1	Amplifier	29
Fig.2-1-2	Triming Resistor	30
Fig.2-2	VREF2 Generator	31
Fig.2-3	IREF2 Generator	32
Fig.2-4	Start-up	33
Fig.2-5	Hys-INV	34

Fig.3	UVLO Thermal Shutdown Block	35
Fig.3-1	Under Voltage Detector	36
Fig.3-1-1	Comparator1	37
Fig.3-2	Thermal Sensor	38
Fig.3-2-1	Thermal Detector	39
Fig.3-3	Reset Control	40
Fig.4	FB Voltage Divider	41
Fig.4-1	FB Resistance Control	42
Fig.4-2	FB Resistor	43
Fig.4-3	FB Detector	44
Fig.5	PFM Comparator Block	45
Fig.5-1	Bias Generator1	46
Fig.5-2	PFM Comparator	47
Fig.6	PWM Comparator Block	48
Fig.6-1	Bias Generator2	49
Fig.6-2	Bias Generator3	50
Fig.6-3	Control Circuit1	51
Fig.6-4	IDAC	52
Fig.6-5	Bias Generator4	53
Fig.6-6	SW Input	54
Fig.6-7	PWM Comparator	55
Fig.6-8	Timer Circuit	56
Fig.6-9	Delay Circuit	57
Fig.7	Driver Control	58
Fig.7-1	Syncro Start	59
Fig.7-2	Control Circuit2	60
Fig.7-3	Selector1	61
Fig.7-4	Control Circuit3	62
Fig.7-5	High-Side PreDriver1	63
Fig.7-6	High-Side PreDriver2	64
Fig.7-7	Low-Side PreDriver1	65
Fig.7-8	Low-Side PreDriver2	66
Fig.7-9	SW Power Control	67
Fig.7-10	PreDriver Control	68
Fig.8	Output Driver	69
Fig.9	Current Limit Detect	70
Fig.9-1	Bias Generator5	71
Fig.9-2	Current Sense	72
Fig.9-2-1	Current Control	73
Fig.9-2-2	Current Sink1	74
Fig.9-3	Current Sense Amplifier	75
Fig.9-4	Current Limit Detector	76

Fig.10	Negative Inductor Current Detect	77
Fig.10-1	Control Circuit4	78
Fig.10-2	Control Circuit5	79
Fig.10-3	Pulse Generator1	80
Fig.10-4	Bias Generator6	81
Fig.10-5	SW Current Detector	82
Fig.10-5-1	Current Sink2	83
Fig.10-6	Pulse Generator2	84
Fig.10-7	Current Detect Buffer	85
Fig.11	Control Logic	86
Fig.11-1	Logic1 BLK7	87
Fig.11-1-1	Logic1 BLK5	88
Fig.11-1-1-1	L1 2Bit Counter1	89
Fig.11-1-1-2	L1 Logic3	90
Fig.11-1-1-3	L1 Logic2	91
Fig.11-1-1-4	L1 Syncronizer1	92
Fig.11-1-1-5	L1 Logic1	93
Fig.11-1-2	Logic1 BLK3	94
Fig.11-1-2-1	L1 Clock Gate	95
Fig.11-1-2-2	L1 8Bit Counter	96
Fig.11-1-2-3	L1 Redactance	97
Fig.11-1-2-4	L1 2Bit Counter2	98
Fig.11-1-3	Logic1 BLK2	99
Fig.11-1-3-1	L1 6Bit Counter	100
Fig.11-1-3-2	L1 Encoder	101
Fig.11-1-3-3	L1 Decoder+Latch1	102
Fig.11-1-3-4	L1 Decoder+Latch2	103
Fig.11-1-3-5	L1 Decoder+Latch3	104
Fig.11-1-3-6	L1 Decoder+Latch4	105
Fig.11-1-3-7	L1 Selector2	106
Fig.11-1-3-8	L1 Wired-nor	107
Fig.11-1-3-8-1	L1 Wired-nor Block	108
Fig.11-1-3-8-1-1	L1 Wired-nor cell1	109
Fig.11-1-3-8-1-2	L1 Wired-nor cell2	110
Fig.11-1-3-9	L1 Decoder	111
Fig.11-1-4	L1 Logic9	112
Fig.11-2	Logic1 BLK4	113
Fig.11-2-1	L1 Logic5	114
Fig.11-2-2	L1 Timing Selector	115
Fig.11-2-3	L1 Logic8	116

Fig.11-3	Logic1 BLK1	117
Fig.11-3-1	L1 Logic7	118
Fig.11-3-2	L1 Logic6	119
Fig.11-3-3	L1 Syncronizer2	120
Fig.11-3-4	L1 Logic4	121
Fig.11-3-5	L1 Divider1	122
Fig.11-4	L1 EN Input Control	123
Fig.11-5	L1 Latch	124
Fig.11-6	Logic1 BLK6	125
Fig.11-7	L1 SW Control	126
Fig.11-7-1	MODE Input	127
Fig.12	Frequency Control	128
Fig.12-1	Logic2 BLK17	129
Fig.12-3	CLK Generator	131
Fig.12-4	Logic2 BLK19	132
Fig.12-5-1	Shift Register1	133
Fig.12-5-2	Shift Register2	134
Fig.12-6	Frequency Detect	135
Fig.12-7	Logic BLK20	136
Fig.12-8	Shift Register3	137
Fig.12-9	Logic BLK21	138
Fig.12-10	Logic BLK22	139
Fig.12-11	Logic BLK23	140
Fig.13	Oscillator	141
Fig.13-1	OSC Cotrol	142
Fig.13-2	DAC	143
Fig.13-2-1	Voltage Control	144
Fig.13-3	RC Delay	145
Fig.13-4	Comparator3	146
Fig.13-4-1	Bias Generator7	147
Fig.13-5	Divider2	148
Fig.13-6	Pulse Generator3	149
Fig.13-7	CLK Gate	150
Fig.14	EEPROM Block	151
Fig.14-1	Charge Pump	152
Fig.14-1-1	CP cell	153
Fig.14-2	EEPROM	154
Fig.15	MODE Input Circuit	155
Fig.15-1	Circuit	156
Fig.15-2	Mode Test	157
Fig.15-3	MODE Buffer	158
Fig.15-4	VIN EDS Protection	159

Fig.16	Soft Start	160
Fig.16-1	Counter Control	161
Fig.16-2	4Bit Counter	162
Fig.16-3	Output Circuit	163
Fig.17	EN Input Buffer	164
Fig.17-1	EN EDS Protection	165
	cascode_mos	166
	res1-2s-p	167
	res1-3s-p	168
	res1-4s-p	169
	res1-5s-p	170
	res1-6s-p	171
	res1-7s-p	172
	res1-8s-p	173
	res1-9s-p	174
	res1-10s-p	175
	res1-11s-p	176
	res1-12s-p	177
	res1-13s-p	178
	res1-17s-p	179
	res1-18s-p	180
	res1-27s-p	181
	res1-30s-p	182
	res1-65s-p	183
	res1-80s-p	184
	inv1-1	185
	inv1-p	186
	inv2-p	187
	inv3-p	188
	buf1-p	189
	inv-cki_1-p	190
	nand2_1-1	191
	nand2_1-p	192
	nand2_3-p	193
	nand3_1-p	194
	nand4_1-p	195
	nor2_1-p	196
	nor3_1-p	197
	nor4_1-p	198
	and2_1-1	199
	and2_1-2	200
	and4_1-1	201
	or2_1-1	202
	xor1	203

tg_1-1-p	204
tg_1-p	205
hys_inv1-1	206
hys_inv1-2	207
hys_inv1-3	208
hys_inv1-4	209
hys_inv1-5	210
hys_inv1-6	211
hys_inv1-7	212
dff-pc-nr-1	213
dff-pc-nr-ns-1	214
dff-pc-ns-1	215
mux-1	216
mux-2	217
mux-3	218
mux-4	219
Tie_cell-1	220
Tie_cell-2	221
Tie_cell-3	222
Tie_cell-4	223
L_INV-1	224
L_INV-2	225
L_INV-3	226
L_INV-4	227
L_BUFF-1	228
L_BUFF-2	229
L_BUFF-3	230
L_NAND2-1	231
L_NAND2-2	232
L_NAND2-3	233
L_NAND2-4	234
L_NAND3-1	235
L_NAND3-2	236
L_NAND3-3	237
L_NAND3-4	238
L_NAND4-1	239
L_NAND4-2	240
L_NOR2-1	241
L_NOR2-2	242
L_NOR2-3	243
L_NOR2-4	244
L_NOR2-5	245
L_NOR2-6	246
L_NOR2-7	247

L_NOR3-1	248
L_NOR3-2	249
L_NOR3-3	250
L_NOR4-1	251
L_AND2-1	252
L_AND2-2	253
L_AND2-3	254
L_AND2-4	255
L_AND2-5	256
L_AND2-6	257
L_AND3-1	258
L_AND3-2	259
L_AND4-1	260
L_OR2-1	261
L_OR2-2	262
L_OR2-3	263
L_OR2-4	264
L_OR2-5	265
L_OR2-6	266
L_OR3-1	267
L_OR4-1	268
L_OR4-2	269
L_XNOR2-2	270
L_XOR2-1	271
L_AND-NOR3-1	272
L_AND-NOR4-1	273
L_AND-NOR4-2	274
L_AND-NOR5-1	275
L_AND-NOR6-1	276
L_AND-NOR8-1	277
L_AND-OR-NAND4-1	278
L_AND-OR-NAND4-2	279
L_AND-OR-NAND5-1	280
L_OR-NAND3-1	281
L_OR-NAND3-2	282
L_OR-NAND4-1	283
L_OR-NAND5-1	284
L_OR-NAND6-1	285
L_OR-AND-NOR4-1	286
L_DFF-PC-NR-1	287
L_DFF-PC-NR-2	288
L_DFF-PC-NR-NE-1	289
L_DFF-PC-NR-NS-1	290

L_RS-FF-1	291
L_RS-FF-2	292
L_MUX-1	293
L_MUX-2	294
L_TIE-cell-1	295
L_TIE-cell-2	296
LOGIC-cell-1	297
LOGIC-cell-2	298
LOGIC-cell-3	299

Table1 Chip Information

Product	XA, X-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER
Model Number	XXXXX
Maker	XXXXX
Package Type	6-pin CSP
Package Marking	XXXXX
Chip Marking	XXXXX
Chip Size	1.29mm X 0.93mm = 1.20mm ²
Process	3Metal-2Poly
Process Type	BiCMOS
Gate Length	0.5um

Introduction

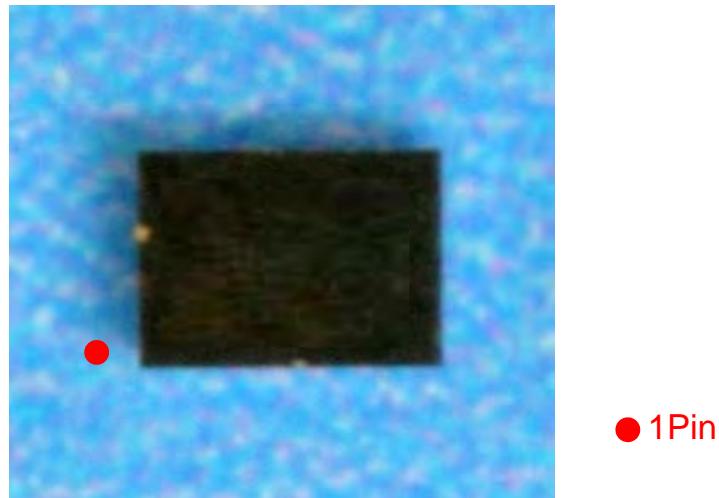


Photo.1-1 Package (Top View)

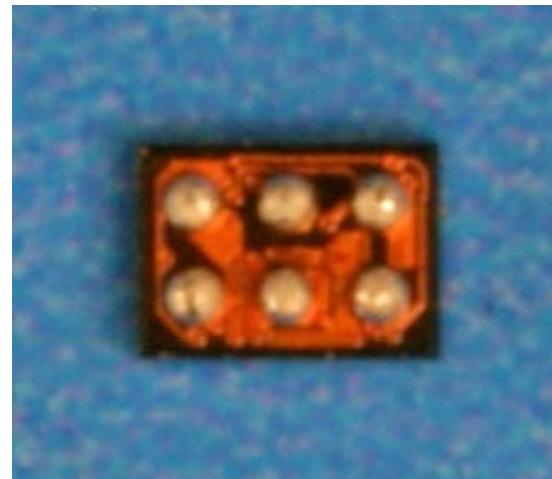
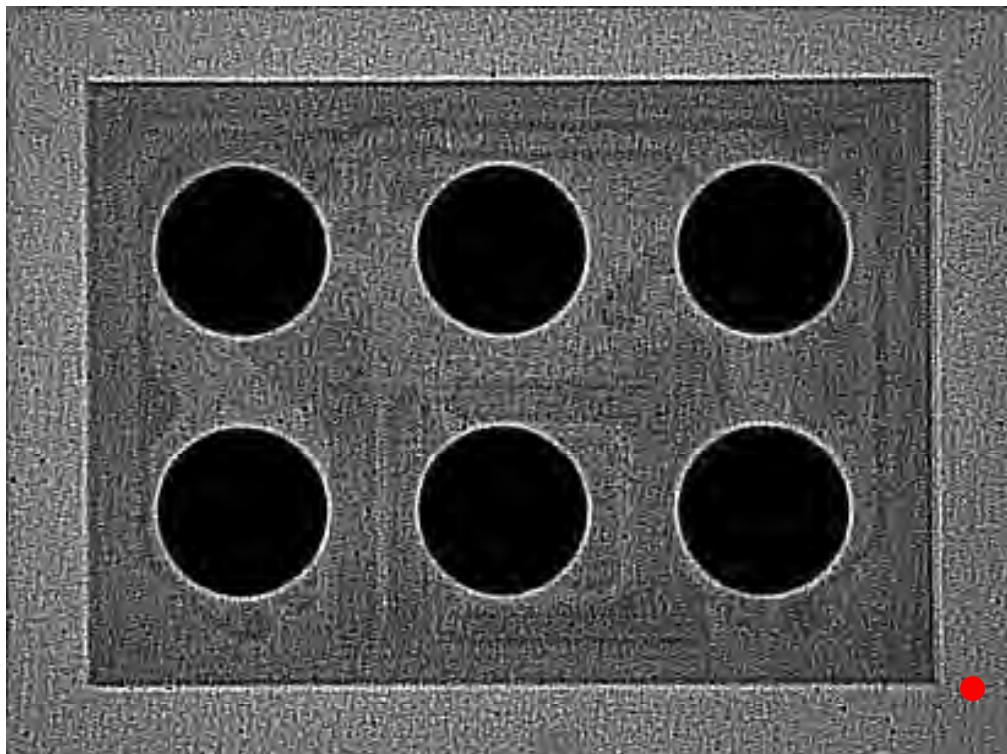


Photo.1-2 Package (Bottom View)

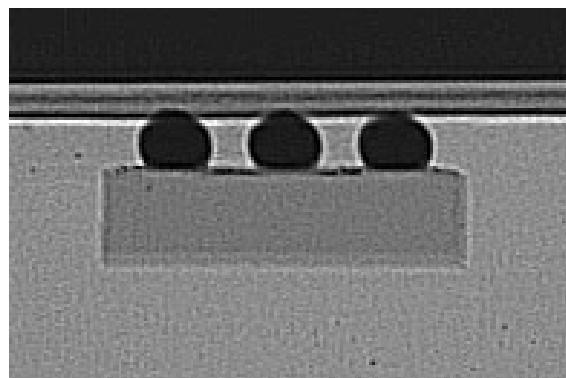


● 1Pin



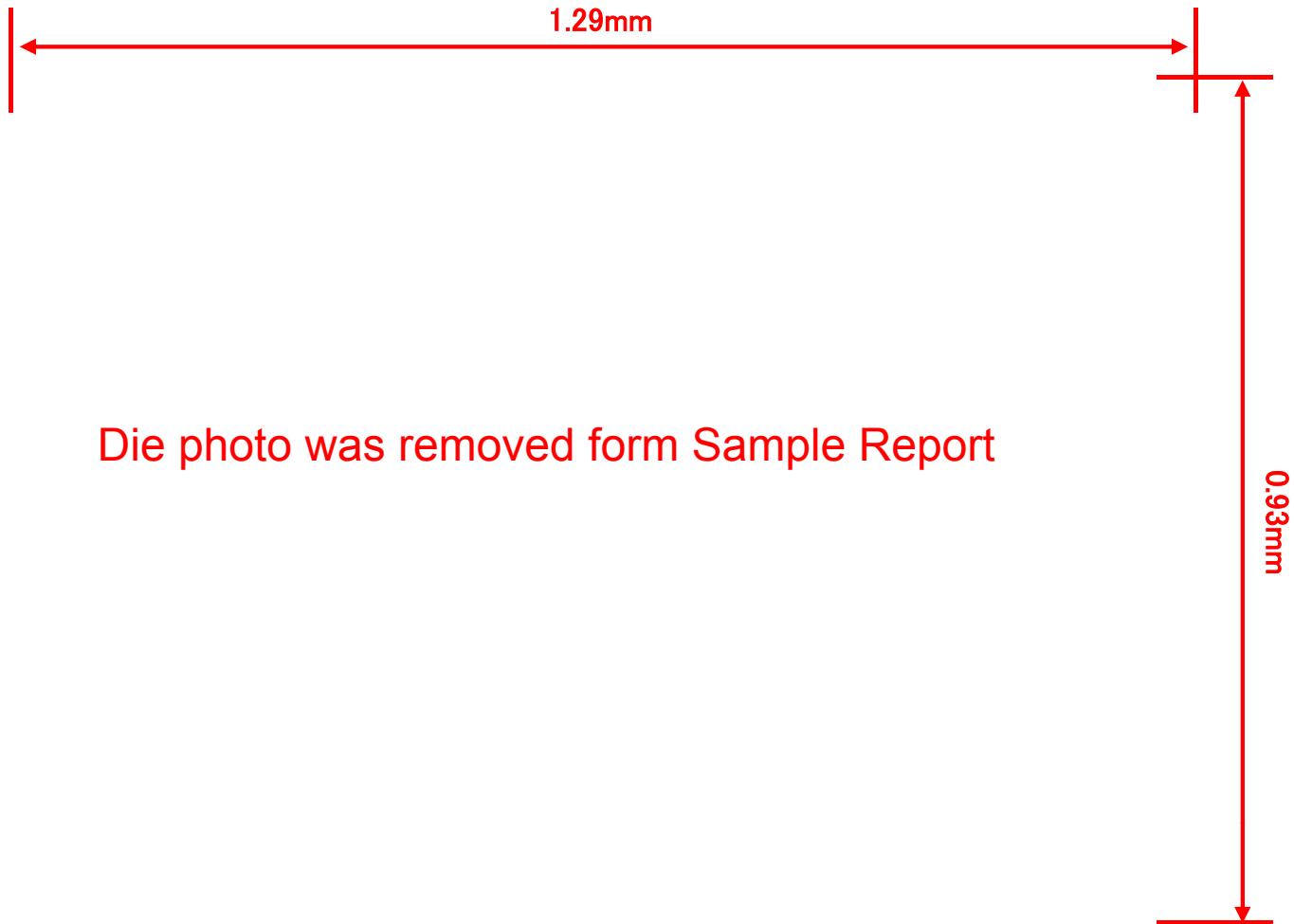
Side View

(Bottom View)



(Side View)

Photo.2 X-Ray



Die photo was removed from Sample Report

Photo.3-1 Chip Overview

1

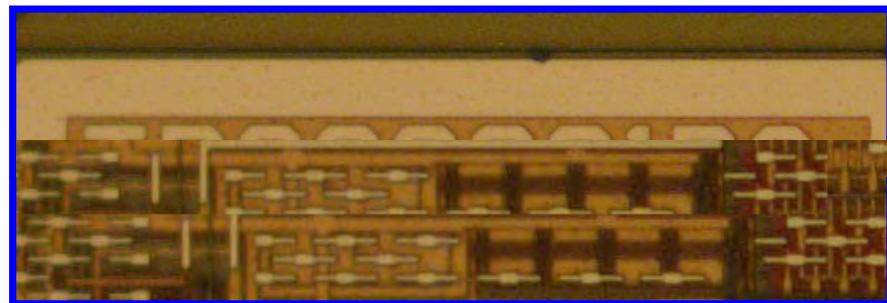


Photo.3-2 Chip Marking1

2



Photo.3-3 Chip Marking2

Pin assignment was removed from Sample Report

Photo.4-1 Pin Assignment (Bottom View)

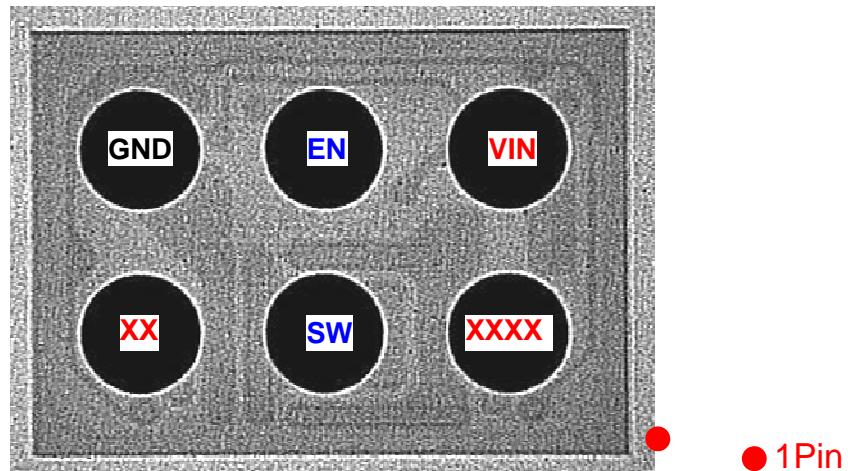


Photo.4-2 Pin Assignment (X-Ray)



GND EN VIN

VIN

GND

VIN

Die photo was partially removed form Sample Report

VIN

GND

SW

GND

VIN

GND FB VIN MODE GND

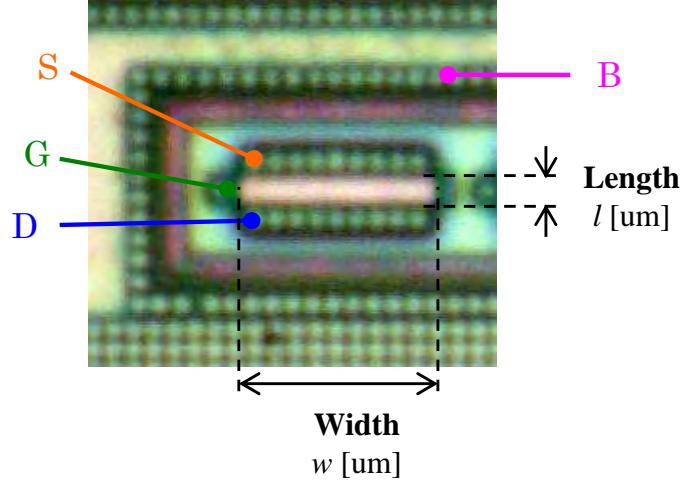


3Metal Layer

Photo.4-3 Pin Assignment (Chip Overview)

Elements

Layout

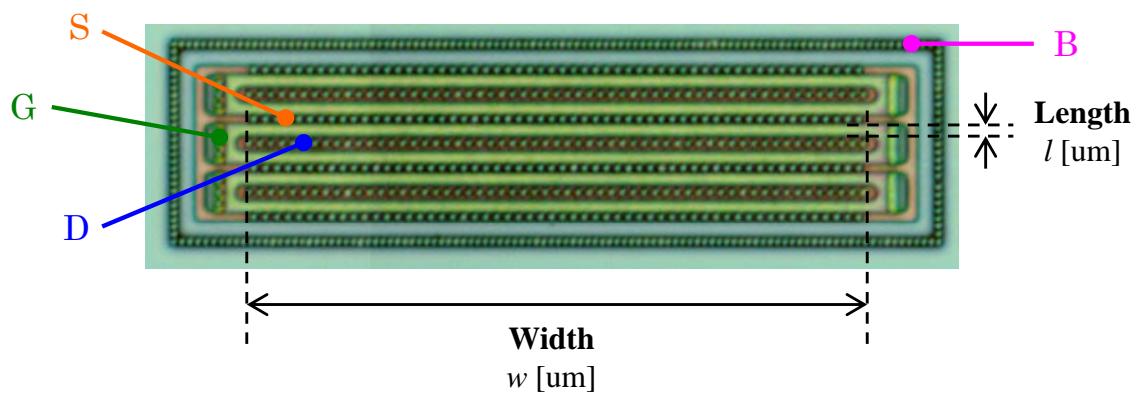


Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol	
[PMOS]				
mfetp4-1		M _n W=w u L=l u M=m mfetp4-1		M _n W=w u L=l u M=m B=body mfetp3-1
mfetn4-1		M _n W=w u L=l u M=m mfetn4-1		M _n W=w u L=l u M=m B=body mfetn3-1

n : element number
m : multiplier
body : body node

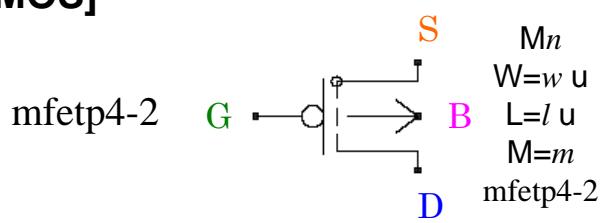
Photo.5-1 MOS Transistor1

Layout

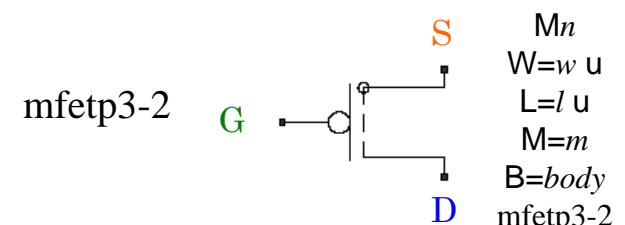


Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol
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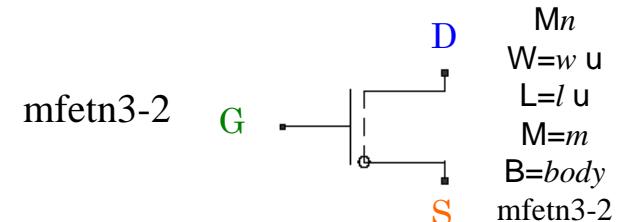
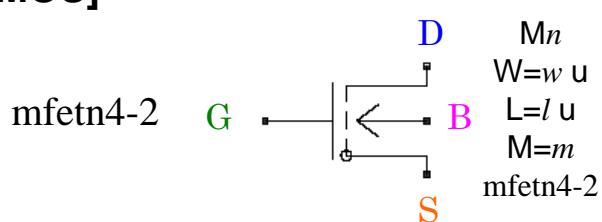
[PMOS]



Cell Name (3 terminal)	Symbol
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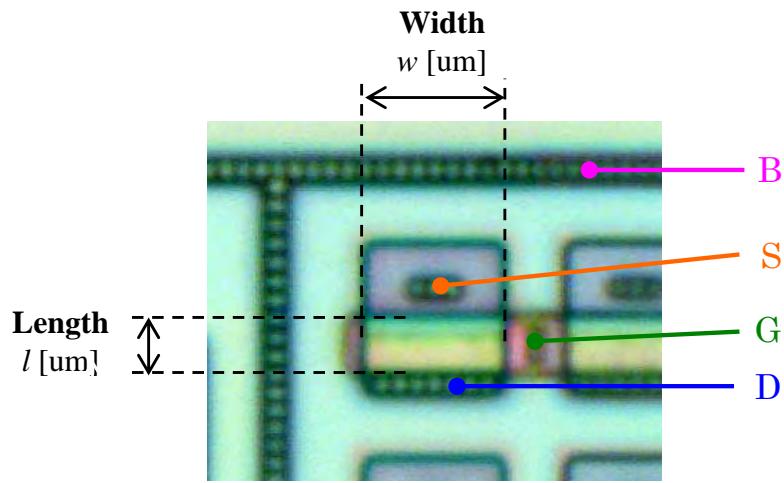


[NMOS]



n : element number
 m : multiplier
 $body$: body node

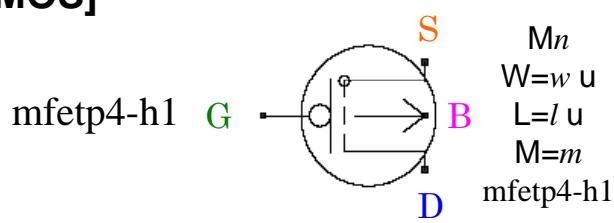
Layout



**Cell Name
(4 terminal)**

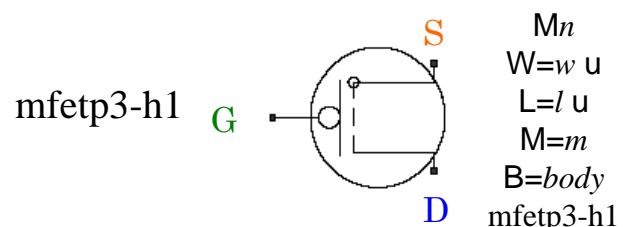
Symbol

[PMOS]

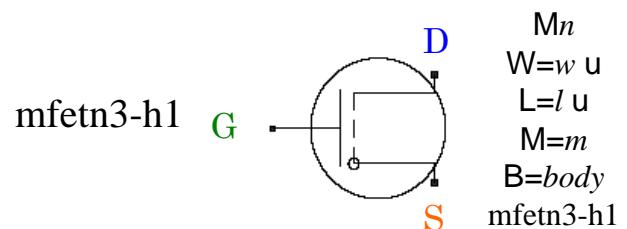
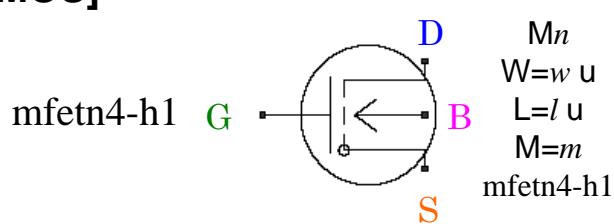


**Cell Name
(3 terminal)**

Symbol



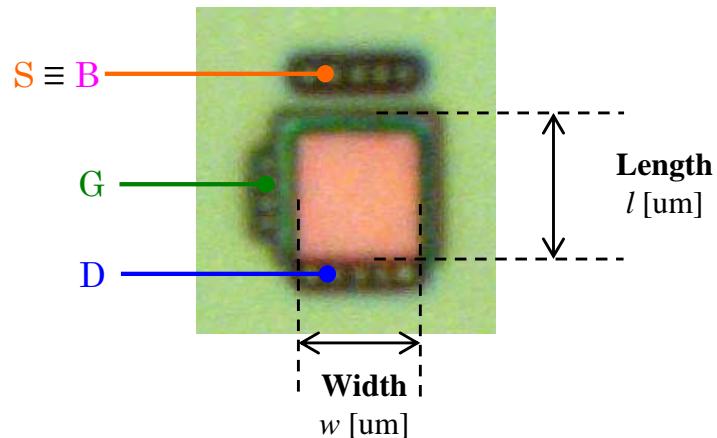
[NMOS]



n : element number
m : multiplier
body : body node

Photo.5-3 HV-MOS Transistor1

Layout



Cell Name (4 terminal)	Symbol	Cell Name (3 terminal)	Symbol
[PMOS]			
mfetp4-h2	 M_n $W=w$ u $L=l$ u $M=m$ mfetp4-h2	mfetp3-h2	 M_n $W=w$ u $L=l$ u $M=m$ $B=body$ Mfetp3-h2
[NMOS]			
mfetn4-h2	 M_n $W=w$ u $L=l$ u $M=m$ Mfetn4-h2	mfetn3-h2	 M_n $W=w$ u $L=l$ u $M=m$ $B=body$ Mfetn3-h2

n : element number
 m : multiplier
 $body$: body node

Photo.5-4 HV-MOS Transistor2

Layout	Cell Name	Symbol
	bjtn-1	<p> Q_n $AREA = w * l \text{ } \mu\text{m}$ $M = m$ </p>

Photo.5-5 Bipolar Transistor

Layout	Cell Name	Symbol
	res1	<p> POLY1 $W = w \text{ } \mu\text{m}$ $L = l \text{ } \mu\text{m}$ $M = m$ </p>

Photo.5-6 Resistor1

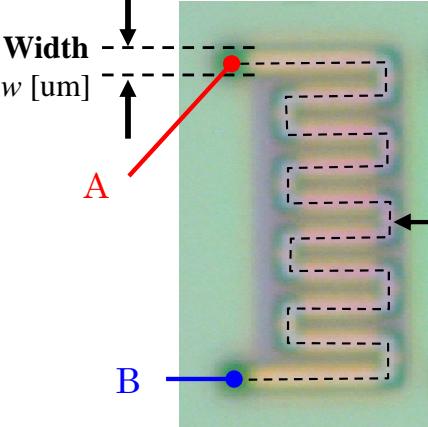
Layout	Cell Name	Symbol
 <p>Width w [um] Length l [um]</p>	res2	 A B $W=w$ u $L=l$ u $M=m$ m : multiplier

Photo.5-7 Resistor2

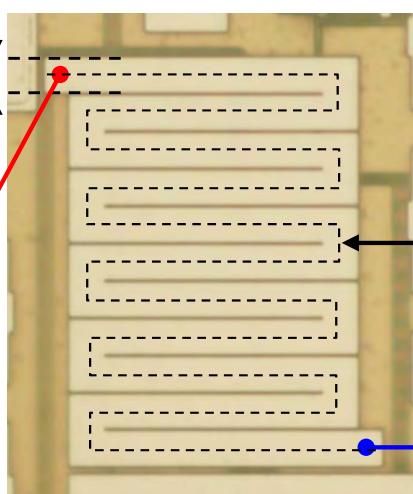
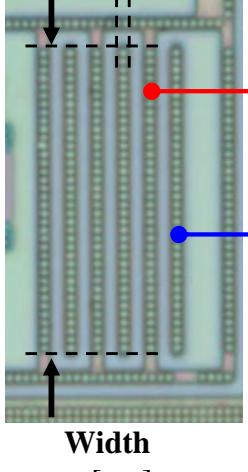
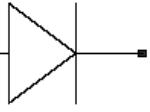
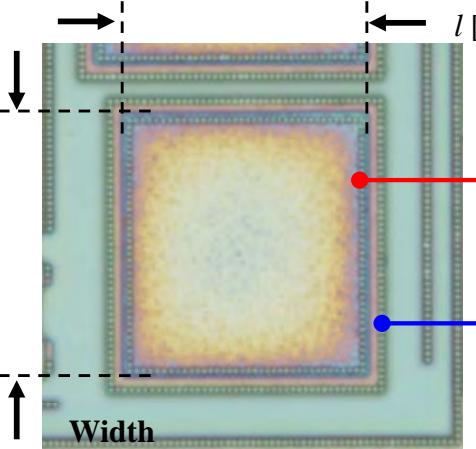
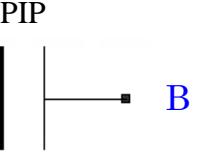
Layout	Cell Name	Symbol
 <p>Width w [um] Length l [um]</p>	res3	 A B $W=w$ u $L=l$ u $M=m$ m : multiplier

Photo.5-8 Resistor3

Layout	Cell Name	Symbol
 <p>Length l [um]</p> <p>Width w [um]</p> <p>A</p> <p>K</p>	dio	 <p>A K</p> <p>$AREA = w * l$ $M = m$</p>

m : multiplier

Photo.5-9 Diode

Layout	Cell Name	Symbol
 <p>Length l [um]</p> <p>Width w [um]</p> <p>A</p> <p>B</p>	cap1	 <p>A B</p> <p>$W = w$ u $L = l$ u $M = m$</p>

n : element number
 m : multiplier

Photo.5-10 Capacitor1

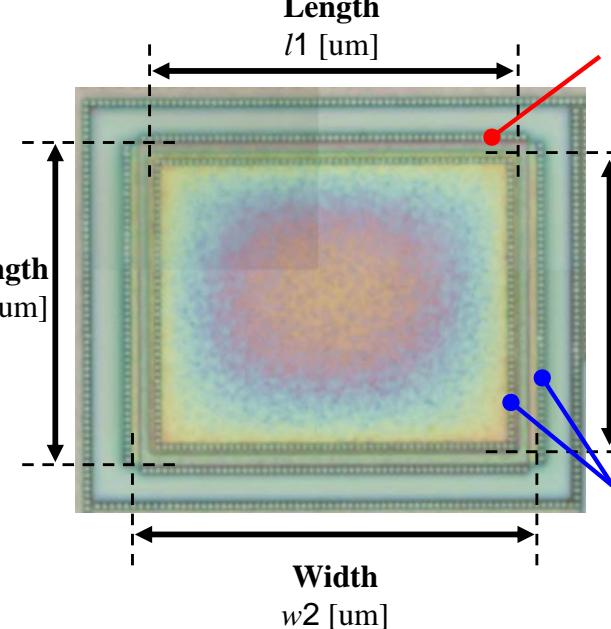
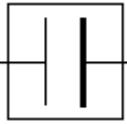
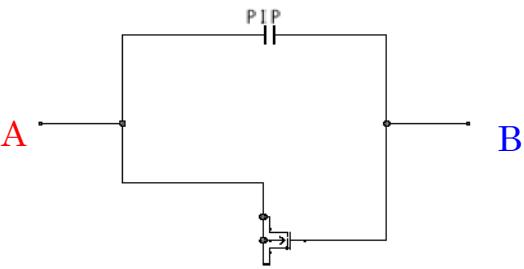
Layout	Cell Name	Symbol
 <p>Length $l1$ [um]</p> <p>Length $l2$ [um]</p> <p>Width $w1$ [um]</p> <p>Width $w2$ [um]</p>	cap2	 <p>A B</p> <p>CW=$w1$ u CL=$l1$ u MW=$w2$ u ML=$l2$ u</p>
Circuit		 <p>A B</p>
CW: Capacitor Width CL: Capacitor Length MW: MOS Capacitor Width ML: MOS Capacitor Length		

Photo.5-11 Capacitor2

Layout	cell name	symbol
<p>Width w_2 [um] Length l_2 [um] Width w_1 [um]</p>	mfetn3-1	 M_n $W=w_1$ u $L=l_1$ u $M=m$ $B=body$ $mfetn3-1$
<p>Width w_2 [um] Length l_2 [um] Width w_1 [um]</p>	cap3	 PID $W=w_2$ u $L=l_2$ u $M=m$

n : element number
 m : multiplier
 $body$: body node

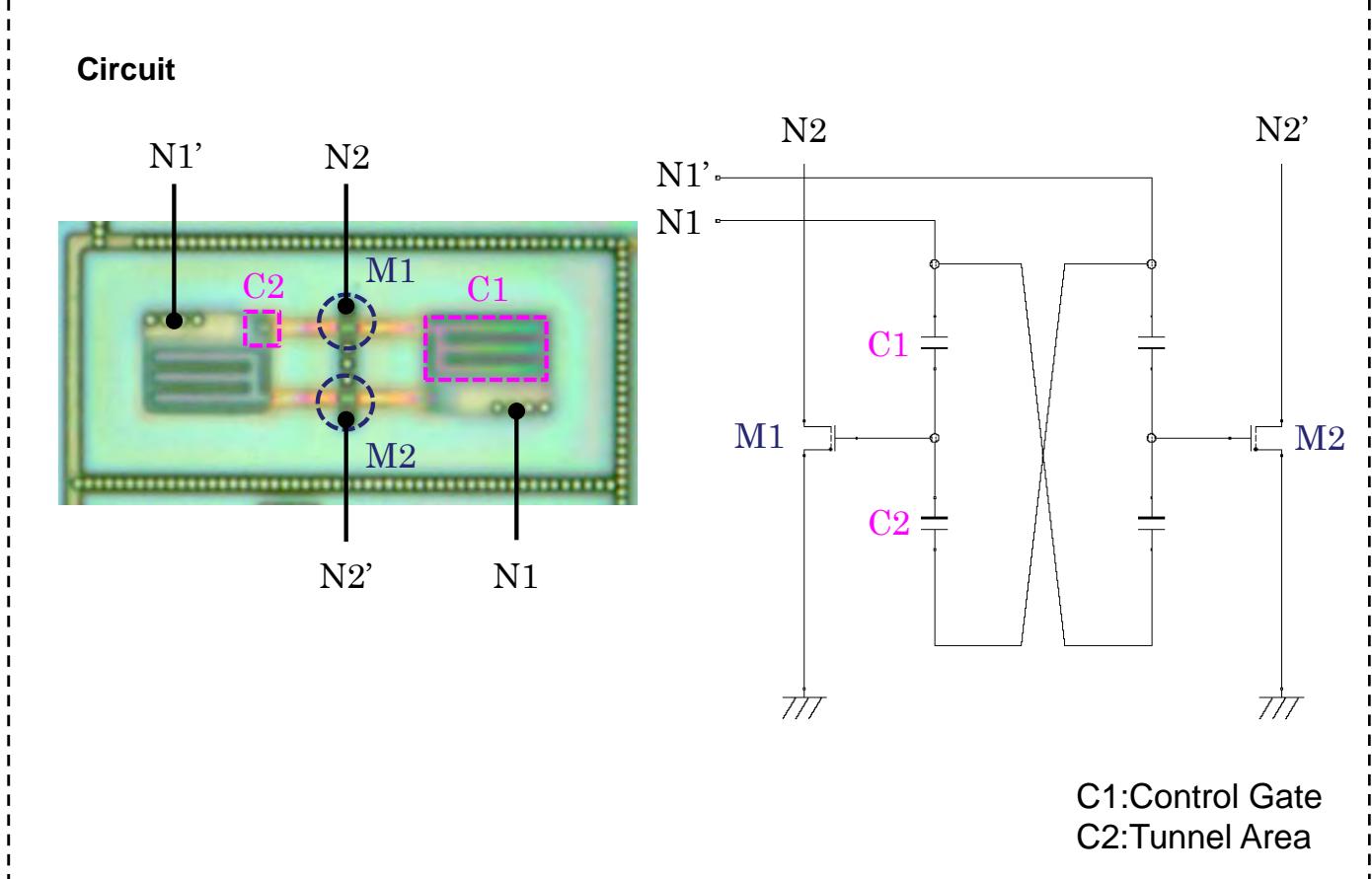


Photo.5-12 EEPROM

Analysis Area Die photo was partially removed form Sample Report

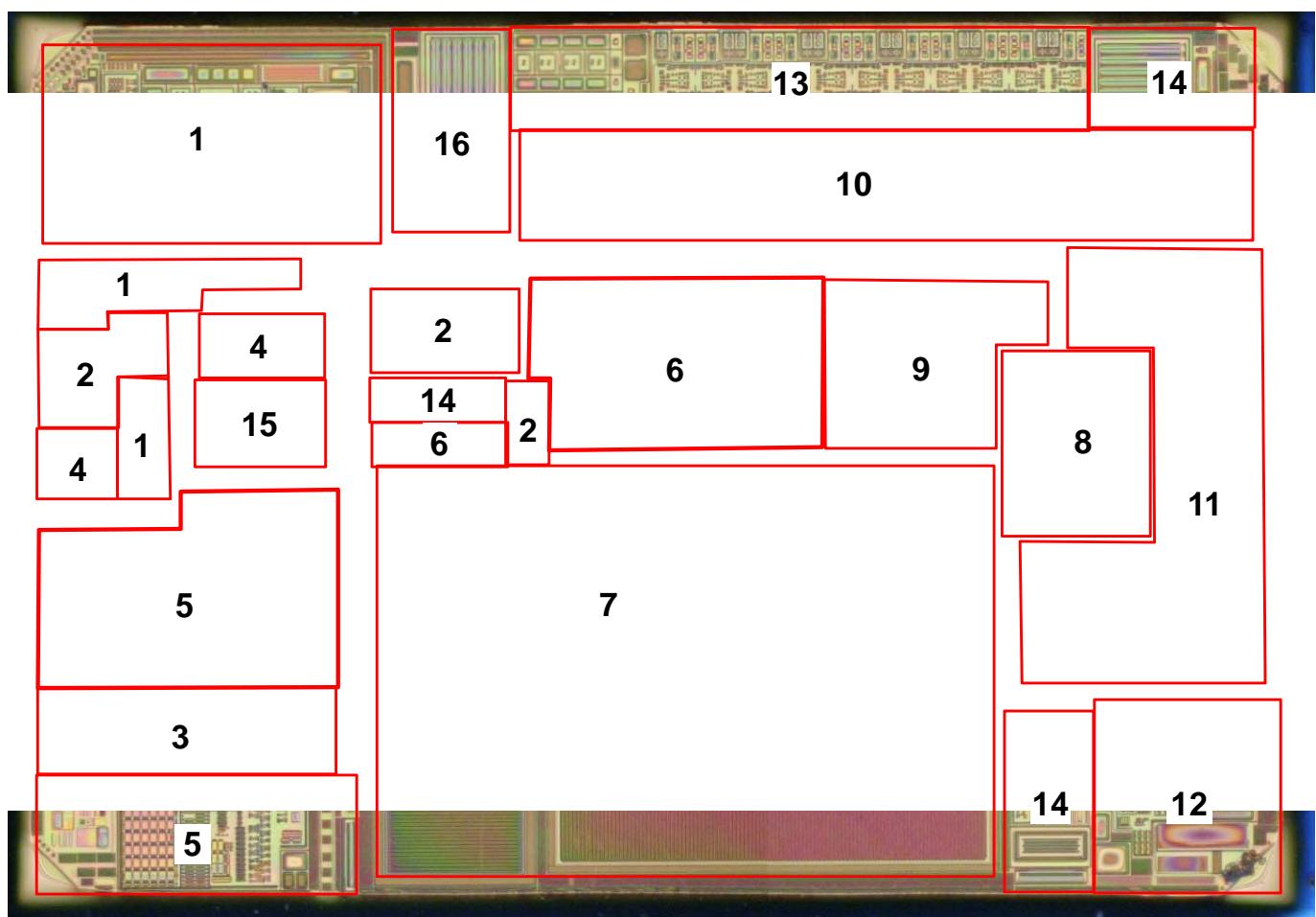


Photo.6 Analysis Area

Table2 Function

No.	Function	Fig.
1	Band-Gap and Bias Supply	Fig.2
2	UVLO Thermal Shutdown	Fig.3
3	FB Voltage Divider	Fig.4
4	PFM Comparator Block	Fig.5
5	PWM Comparator Block	Fig.6
6	Driver Control	Fig.7
7	Output Driver	Fig.8
8	Current Limit Detect	Fig.9
9	Negative Inductor Current Detect	Fig.10
10	Control Logic	Fig.11
11	Frequency Control	Fig.12
12	Oscillator	Fig.13
13	EEPROM Block	Fig.14
14	MODE Input Circuit	Fig.15
15	Soft Start	Fig.16
16	EN Input Circuit	Fig.17

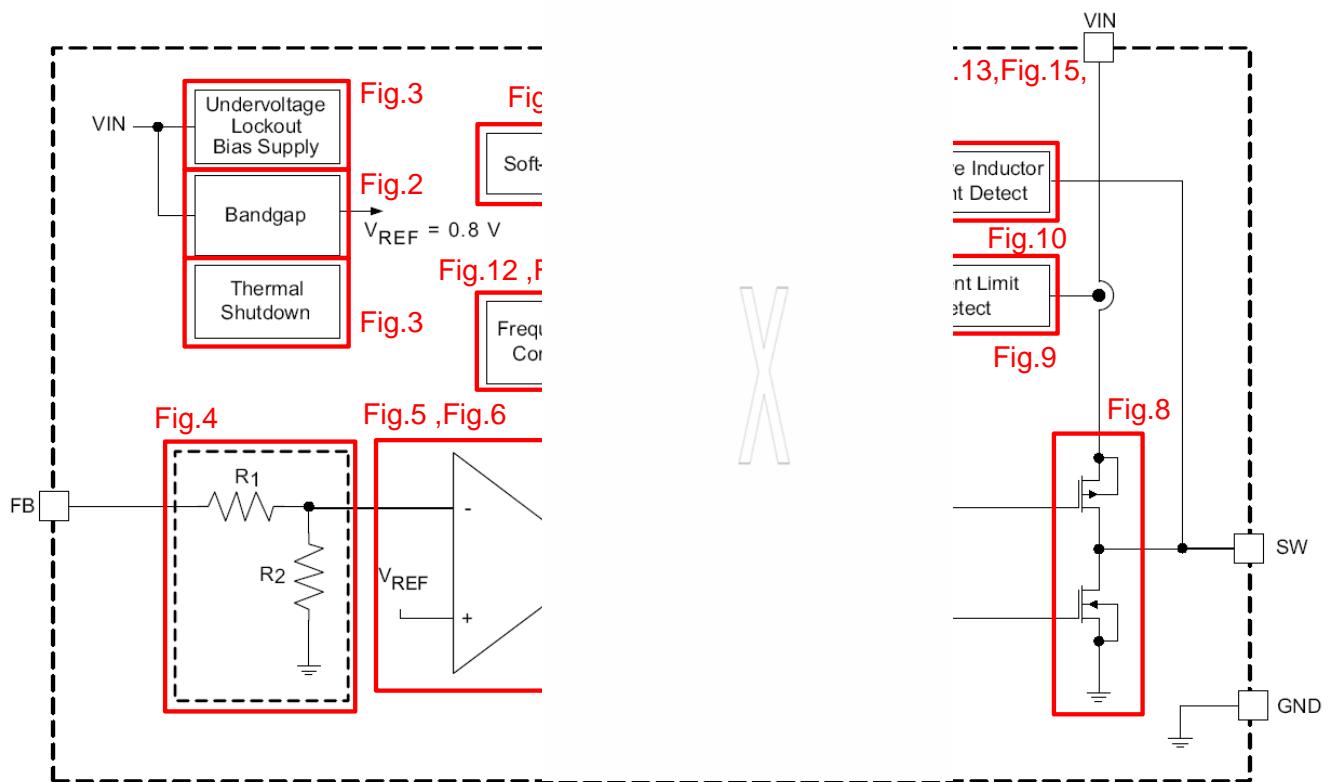


Fig.0 Functional Block Diagram

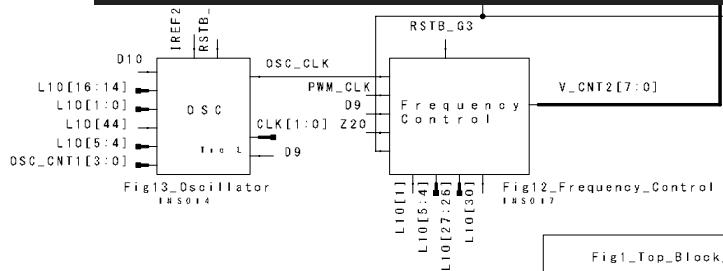
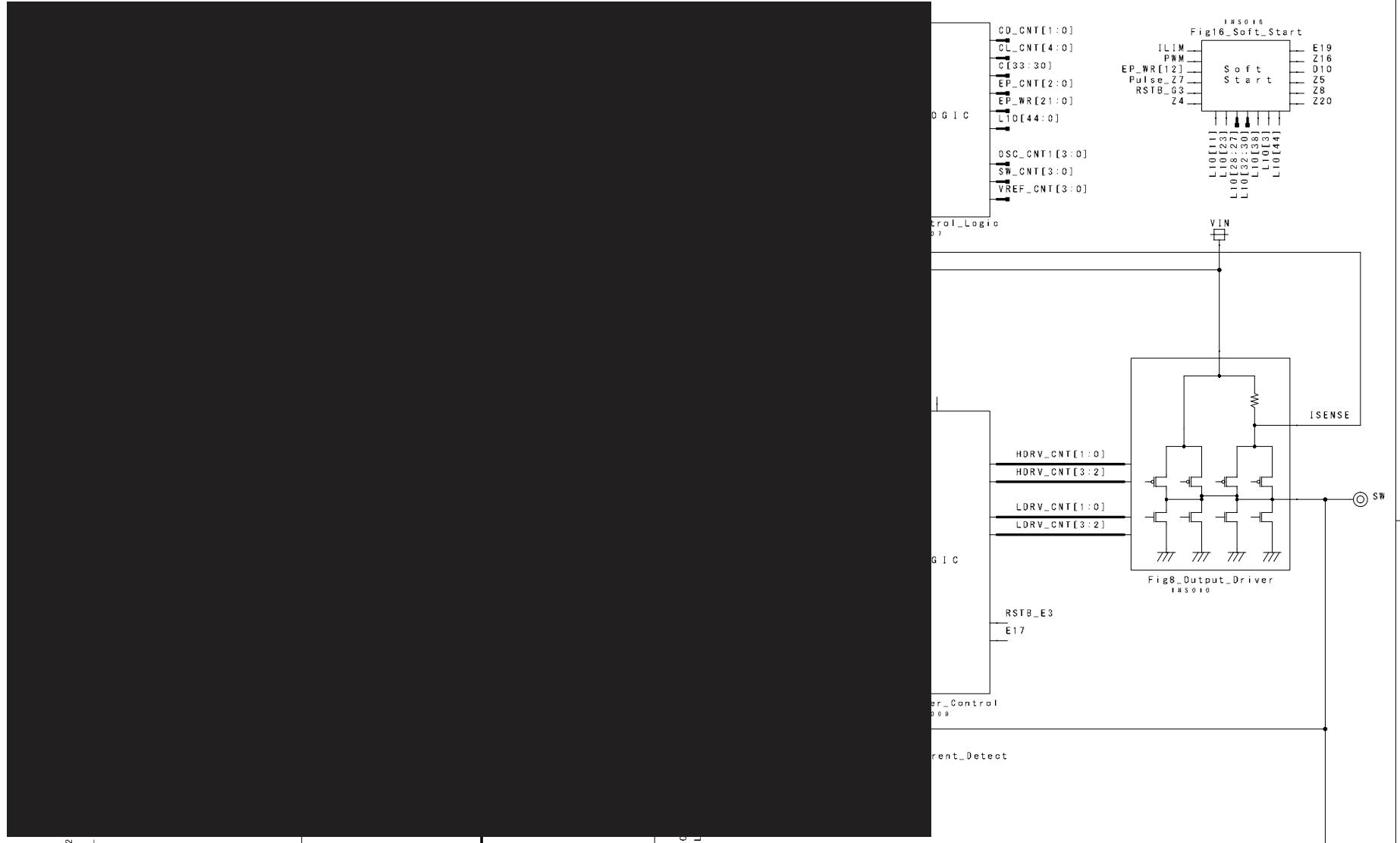
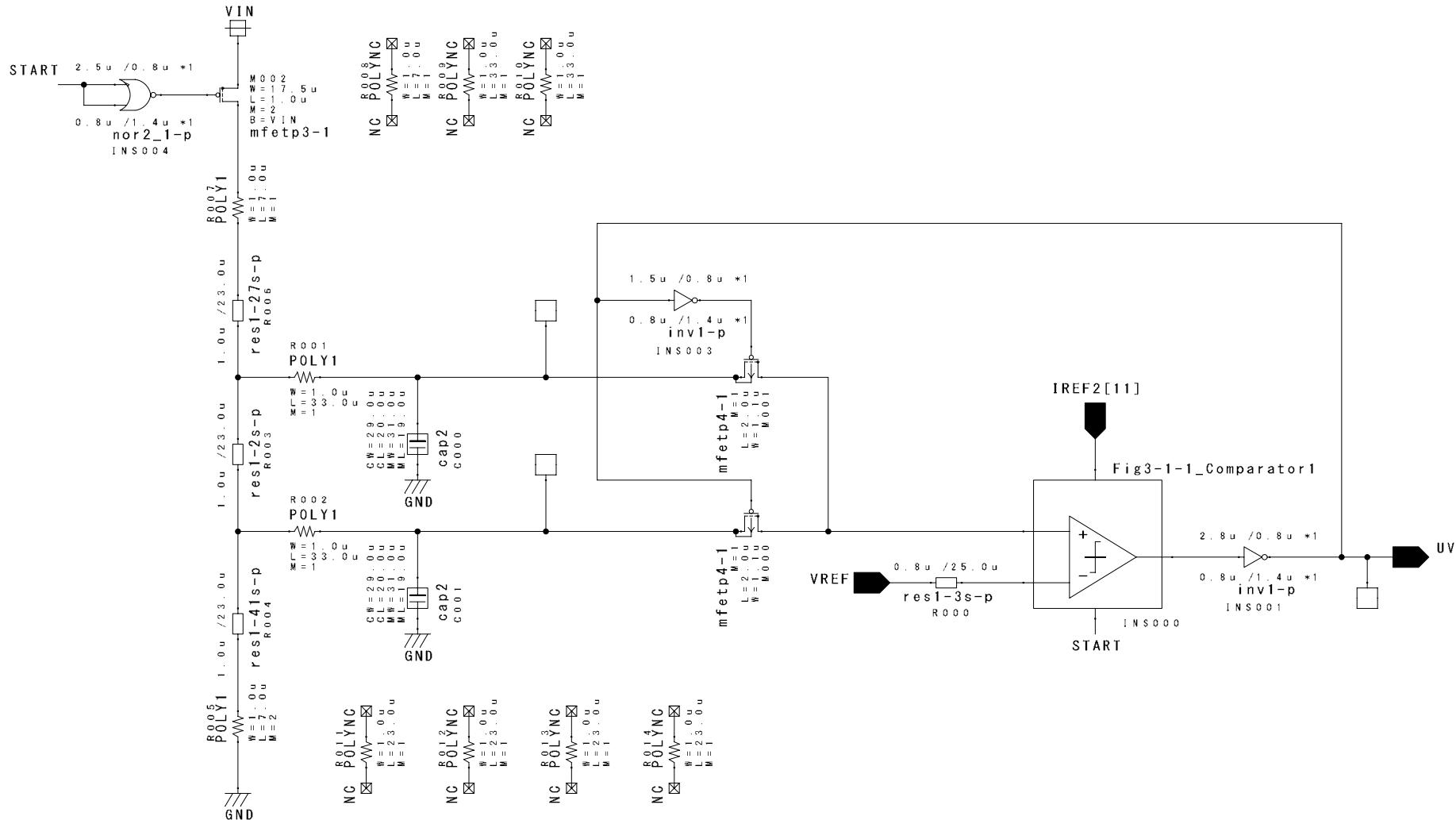


Fig11_Top_Block_Diagram

START



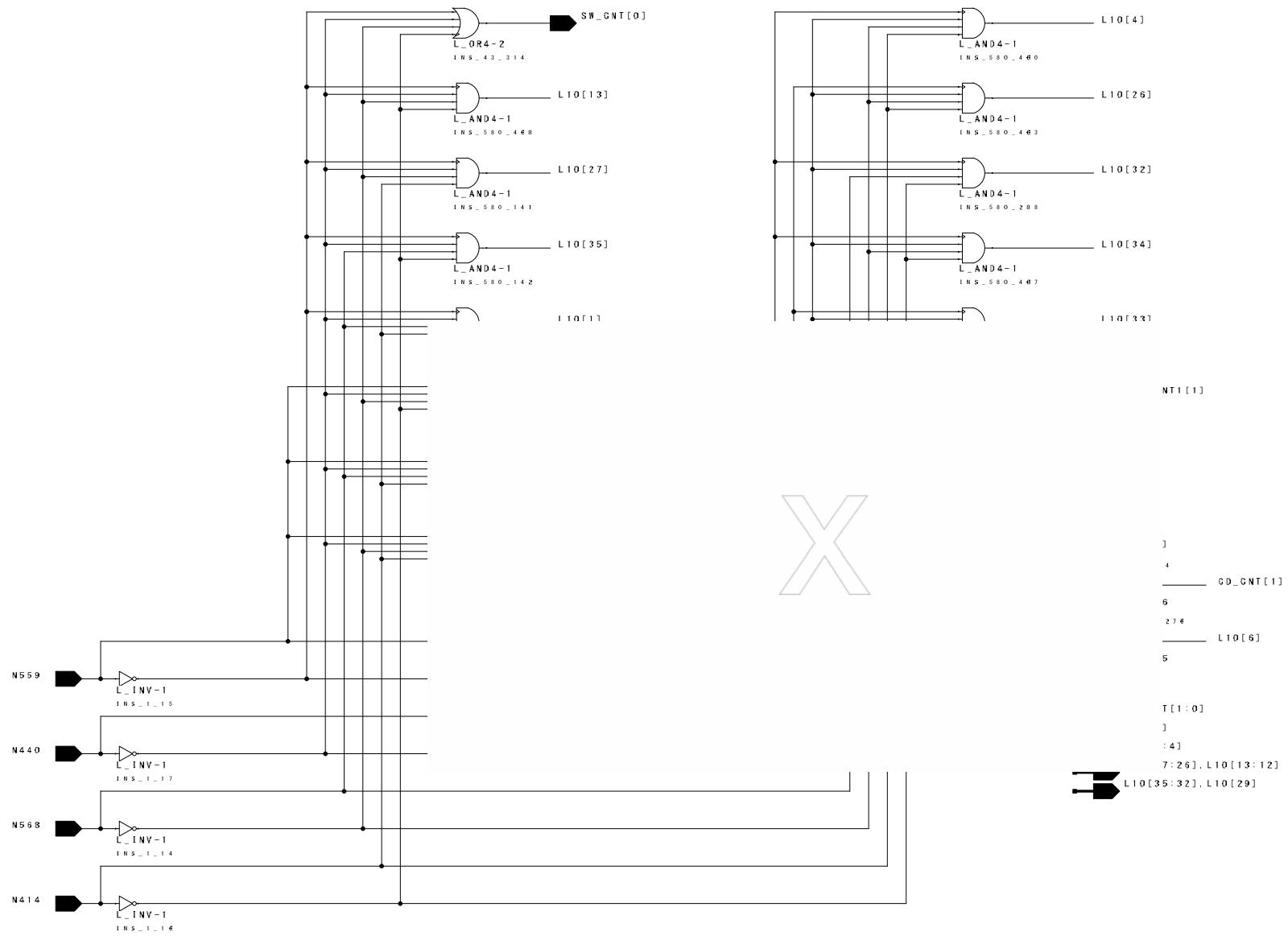
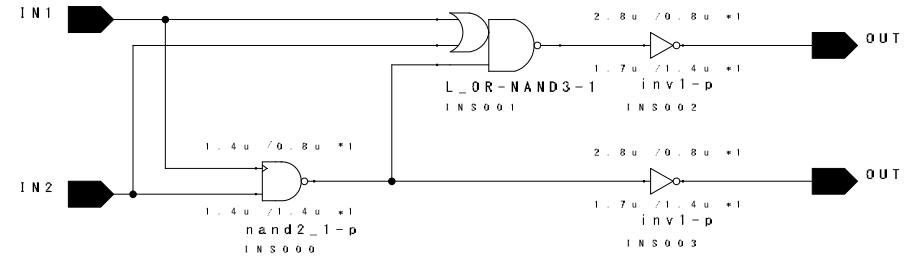


Fig11-1-3-9_L1_Decoder



LOGIC-cell-3

NOTE 000